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The Application of Basic Statistical Sampling and Analysis Techniques to Enhance The Failure Mode Analysis of Electronic Devices.

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by

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ABSTRACT

Functionality data describing the memory cell failure types on an MOS integrated circuit are the focus of a study into improving the analysis and summary of such information. Several sampling techniques are explored to help screen the amount of data that has to be collected or summarized. The various sampling plans are quantitatively compared to one another in order to establish the preferred sampling method.

Basic correlation and analysis of variance procedures are applied against the failure summary data in order to highlight significant failure categories as statistically significant. In addition, trend analysis procedures are outlined that could be used for manufacturing-process monitoring.

The sampling plan that is selected is a form of stratified sampling that tended to provide more insight into product characteristics than any other plan that was examined.

PROJECT INTRODUCTION AND BACKGROUND

Since the advent of the computer and the many advances made on its capabilities man has been developing ever more sophisticated applications for its use. Even in this day and age of the high speed multi-user system and seemingly endless memory capacity one is able to provide an application that overtaxes the equipment that is currently available. What is about to be described in this project is a computer based system that has been over-extended due to the sheer volume of data that is being made available for analysis. What will be studied is an enhanced system based on some simple applications of statistical theory through basic sampling and data analysis routines.

The current system that will be described was in existence two years ago when this project began and any references made refer to that era. The specific values and characteristics of the data do not reflect the actual data from that period nor do they reflect in any way the state of the current technologies. What is important is not the actual data but the statistical data reduction techniques that will be prepared and a judgement as to how well they would work on any set of live or real data.

The system in question supports the failure mode analysis (FMA) procedure for a product engineering group responsible for MOS integrated circuit memory devices. In order to understand the role of the system output which will be influenced by this project's findings, it is necessary to establish a very basic understanding of what the MOS memory device manufacturing cycle comprises and how FMA is performed.

Failure Mode Analysis

Failure Mode Analysis (FMA) in general is the act of determining what is defective with a manufactured product, in our case MOS dynamic memory devices, and then suggesting what the cause of the defect might have been. The next step then is to work with process engineering to rectify the problem. In the integrated circuit business this procedure approaches that of being an art. It is a very complex process just to determine if a device is failing let alone to find out what the failure is and how it was caused. Because of the large number of electronic tests that are performed on any given device the job of analyzing all the data that is available can be extremely formidable.

Not only is the amount of data generated at the various test points extensive, the level of understanding regarding the

manufacturing process from beginning to end that is necessary is extremely comprehensive. When the idea for an FMA system was first developed its intended purpose was to help mechanize some of the thought processes that the product engineer goes through when analyzing product performance data. The ultimate goal would be to attempt to develop an implementation of artificial intelligence by having a computer examine failure data and determine exactly what action needs to be undertaken to rectify the situation. Suffice to say, this first stage of study merely encompasses the reduction of the raw data into a more useable format.

The Manufacturing Process

In order to better understand the goal of FMA it is a good idea to briefly cover the major process steps that an integrated circuit goes through from the formation of the pure silicon material through to the packaging and shipping of the final product. The impact of each step will be discussed as regards to its relation with the FMA procedure.

The first step is, of course, the design of the product. If any deficiencies are accidentally designed into a device they may show up

as hard or soft errors at the end of the manufacturing line. A hard error is one that happens all or a great majority of the time and soft errors are more intermittent but occur often enough to be suspicious. During the course of FMA one may be forced to conclude that there is a flaw in a device design based on the data available. The speed with which one is able to draw this conclusion depends to a large extent on how comprehensive and well presented the information is. The design and re-design of a product is an expensive procedure therefore one must be very sure of a design's contributions to detected failures before implementing a change.

The two criteria then that have to be in balance are the availability of device performance information that is reliable versus the speed and cost of obtaining that data. As will be described, the current system provides reliable data but not in a timely or economically acceptable manner.

The first manufacturing step is the growing of the base silicon material crystal and the slicing of very thin cross-sectional wafers from the final crystalline ingot. The base material's characteristics can have a significant impact on the device's performance. Comprehensive data collection that shows material differences is

vitally important due to the fact that subtle differences in materials from two different sources of supply can have a devastating effect on yield at the end of the line. After the wafer has been created it enters the "wafer fabrication" line. These manufacturing lines are contained within large clean rooms. It is within these clean rooms that wafers go through most of the process steps associated with manufacturing the integrated circuits. In short, the silicon wafer has various layers of semi-conductor material layered one on top of the other until the desired circuit patterns are achieved. Each layer is applied over the entire wafer after which a photolithography operation exposes the circuit pattern through a "mask" thus changing the properties of the exposed versus unexposed material not unlike the exposing of a photographic negative when printing a photograph. The undesired material is then stripped away and the next layer is applied in a similar manner.

This is, of course, an extremely simplistic view of the integrated circuit manufacturing process, but each time the wafer goes through the photolithography and etching steps there is the chance of inducing a defect on any circuit. For example, if the mask used to expose the circuit is defective because it has small particles of dust residing on vital areas then the circuit could be ruined due to variations in the light pattern caused by the dust. Some devices

require many layers of circuits. Thus allowing a high probability of device failure and the low and often erratic yields that are characteristic of this business.

The wafers go through a variety of other process steps before emerging from the clean room. Once the clean room cycle is complete the wafers have many potentially functional devices laid out in an array. While still in this wafer form the devices are tested so that the ones that appear to be functional will be identified before proceeding on to the next step; this is known as the wafer probe operation. In the case of some memory devices, which this study concentrates on, there are actually three test points near the end of the line: (1) laser repair (2) wafer probe and (3) package test. These three points represent the points at which the majority of product performance data is collected for use by the engineering organizations.

Product Engineering Responsibilities

The product engineering group is responsible for the product lines it supports from the standpoint of product design integrity, functionality and quality. A product engineer on an MOS product line has a very complex process to help keep under control. The engineer must have a vast knowledge of what makes a given device work or fail

and how it is manufactured in order to make judgements about the state of health for a single device or an entire product line. One of the greatest frustrations for an engineer, though, is lack of information.

Lack of information does not necessarily equate to lack of data for one could have many stacks of paper filled with data that is just too voluminous to sift through to draw any conclusions from. On the other hand there may be no data available from which to determine how a product is doing. Basic yield and functionality data are always available at the end of the line where the testing takes place. It is at these testing points that most of the data describing a device's characteristics is generated and made available. It is this data and its overwhelming abundance that is the subject of this paper.

The Laser Host System

One of the manufacturing steps that the memory devices go through is called the laser repair operation. It is possible to analyze, with a micro-computer, the functionality of a memory device by reading and writing to all the memory cells on the device. This information is examined and a determination is made regarding the repairability of the device. One can imagine a memory device as one huge matrix into which a series of 1's or 0's can be written by causing the presence or

absence of an eletrical charge. If there are only a few rows or columns in the matrix that do not function correctly, a laser can be used to disable that element and enable a spare row or column. Therefore, a device is considered repairable if there is the right combination of rows and columns that can be enabled and disabled to result in an entire matrix of functional memory cells.

At the time that the laser micro-computer is analyzing a chip site there exists an opportunity to collect all the functionality information regarding each chip site and transmit that data up to a host computer for storage. Subsequent detailed analysis and historical comparisons can then be made. This paper will deal with the analysis of this vast quantity of data that is collected at the laser repair operation and how to better use that data.

The laser host computer system that is in place requires a great deal of application software to sift through all the data collected from each wafer in a lot. The system analyzes all the cell defects and assigns them to one of several pre-determined "failure categories." For example, if several but not all cells in a column or row were bad the failure category counter for a "weak column" or "weak row" would be incremented. All the failure patterns on all the sites are categorized and a summary sheet is generated that shows, for a given wafer, all the

failure types that were observed and on how many chip sites they occured (see Appendix A). With a mini-computer dedicated entirely to this task it takes about eight hours to generate the one summary sheet for a sample of ten wafers from a lot. Any given lot can have as many as 25 wafers in it and there can be several lots being repaired at any one time that are all networked to the host computer. Under current procedures only one lot can be actively engaged at a time for data collection and analysis. The result is that only those lots and wafers singled out for analysis can be analyzed. This leaves a great deal of missed opportunities to measure product quality.

The Objective of This Study

The goal then is to speed up the analysis by employing a statistical sampling plan so that all lots passing through the operation can be sampled and included in an overall measure of the state of any given memory product line. Phase one of this paper deals with the selection of the sampling plan that will help speed up the system analysis time. Phase two will investigate ways of enhancing and aiding the interpretation of the system's output by employing a statistical analysis scheme for the final summary reports. The new summary will help to point out or highlight the significant error types that were observed over any given population of collected data and will be referred to as the "results analysis" section.

CHOOSING THE SAMPLE SIZE

The first step to take towards making the FMA analysis more efficient is to employ some sampling techniques. This would reduce the amount of data that needs to be analyzed and thus shorten the analysis time. There are two major steps involved in adopting a sampling technique: (1) choosing a sample size and (2) choosing an appropriate method of taking the sample. In the case of this project the sample size refers to the number of chip sites from which one needs to collect individual memory cell functionality data in order to perform a meaningful and representative analysis of any given wafer.

The sample size was examined from two different perspectives. The initial goal of this project was to reproduce the original lot summary intact based on sampled data. It will be shown that this was attempted and subsequently rejected in favor of a modified or reduced lot summary output.

What to Sample For

The first question to answer before the sample size can be determined is what does one want to characterize or predict. The lot summary report as it exists in Appendix A shows not only a lot characterization but also the individual wafer summaries. Secondly, one must determine what parameter is to be estimated.

On any given wafer for the specific product line being examined there are 309 physical chip sites that can comprise the sampling universe for a wafer. This would vary, of course, depending on the product line and wafer size. Based on past history from 100% counts one has an idea of what value to expect for each failure category. For example, the sample lot that is shown in Appendix A shows the row failure category running at about thirteen (13) defects per wafer or about four (4) percent of all the defects. The range for row failures goes from eight (8) to twenty (20) defects and from two (2) to seven (7) percent. It should be noted that the lowest count and lowest percentage do not necessarily occur on the same wafer.

The information that is generally of most interest to the user of this summary is the percentage value (those figures appearing in the parentheses). These figures illustrate how any given defect category

compares to any other or to the overall number of defects. Appendix A shows that fifty-seven percent of all the defects were single bit failures. If this proportion can be accurately estimated based on a sample such that both wafer and lot summaries can be generated, then the essential results of the summary can be determined from sampled data rather than from a comprehensive count. It is the goal of this section of the study to determine what sample size and method is appropriate to accomplish this aim and to decide whether or not both the wafer and the lot summaries can be accurately estimated.

Analyzable Versus Unanalyzable Sites

This particular application of sampling theory is made more complicated by a couple of factors. The first is that one is dealing with a finite universe when taking a sample from a single wafer for there are only 309 available sites from which to choose. The second factor is that not every site that is sampled can be used in the analysis because information is not necessarily available for every site on the wafer. Some sites may have experienced a physical contact failure with the testing equipment and therefore provide no defect information and other sites may have so many failures that the software that has been developed is unable to decipher all the failures and accurately categorize them; these latter sites are labelled as "too

complex" or "pre-screened" failures. The sites providing no information show up as blanks on the wafer maps (Appendix B).

It is felt that from a software standpoint it would be simpler to try and develop a sampling plan that accepted data from the sampled sites over the data link without determining the specific characteristics of each site regarding its analyzability. The data is not transmitted in a form that readily lends itself to real time analysis. It is better to collect all the sampled data at once then examine it to determine its characteristics after the transmission is complete. A prerequisite for this entire system is that the operations of the host computer must be transparent to the laser repair operation. Nothing must jeopardize the capacity of the repair facilities by slowing them down.

Definitions for This Study

The requirement then in terms of choosing a sampling plan is that one must plan ahead for a large enough sample of sites in order to ensure that there are enough analyzable ones in the sample with which to accurately perform the study. As a first step it is important to provide some definitions and try to characterize the situation mathematically.

Definitions: N_i = # of sites examined on wafer "i" to find "n_i" analyzable sites

d_{ik}= # of "k" type defects found over the n_i sites on wafer "i"

C_{ik}= # of "k" defects per usable site on wafer "i" estimated by d_{ik}/n_{ik}

conditions: $C_{ik} \leq 7$
(by definition, no single site can have more than seven defects and still be considered analyzable. This is a system software limitation.)

x_{ijk}= # of "k" defects at site "j" on wafer "i"

u = population mean value for "x"

therefore: $x_{ijk} \leq 7$

$d_{ik} = \text{Sum } x_{ijk} \text{ [from } j=1,\ldots,n_i\text{]}$

$N_i \leq 309$ (for the specific product in question there are only 309 potential sites on the wafer)

M_i = estimate of # of usable sites on wafer "i" = $(309n_i)/N_i$

The First Sample Size Determination

If $V(u) = \frac{s^2}{n}\frac{(N-n)}{N-1}$ where N = population size, n = sample size Eq[A][1]

Note: The factor (N-n)/(N-1) is the finite population correction factor.

one can solve for "n" as follows:

$$n = \frac{Ns^2}{(N-1)\,V(u)+s^2} \qquad \text{Eq[B]}$$

[1]William G. Cochran, Sampling Techniques, (John Wiley & Sons, Inc., New York, 1964), p.23

Given the above equation and definition one can now attempt to determine the appropriate sample size for this study. All that is required is the application of some "live" data based on current conditions.

If from past experience it is known that the standard deviation for the number of failures associated with the single bit category ranges between 1.5 and 1.9 and the mean for the single bit defect type is about 0.6 per site, then one can substitute into equation [B] to determine sample size . Using a standard deviation that is based on +/- 10% of the mean to give the desired variance the sample size calculates as follows:

$$n = \frac{309\ (1.5)^2}{308(.06)^2 + (1.5)^2} = 207 \text{ sites}$$

Therefore, if one wanted the standard deviation of the mean of the sample to be no greater than ten percent of the mean one should choose a sample size on the order of 207 or about 66 percent of all the sites on the wafer. This would only be a good sample size for the case of single bit defects. If one were to examine the situation for a defect type that occurs with less frequency it would look as follows:

mean defects/site (row failures) = 0.04

$s^2 = .081$

$$\text{then } n = \frac{309\ (.081)}{308(.004)^2 + (.081)} = 292$$

A sample of 292 sites out of a population of 309 essentially constitutes a 100% count and therefore would provide no savings for the laser host system.

The Chosen Sample Size

In order to gain an understanding of the data being dealt with it was decided to go ahead and pick a convenient sample size and see what results occured. The sample size was chosen for testing purposes based on initial understandings of sampling theory. For a variety of reasons, one of which was convenience, a sample size of 55 sites was used in the early stages to test out various methods. Once the sampling plans had been fully developed new samples should have been taken with the proper sizes but time pressures precluded any additional studies. Therefore, the sample size of approximately 55 sites will be used several times in this study when investigating the merits of each plan examined. By using equation [A] from above, one can calculate the expected variance of such a sample. Such a sample size should give the following variance:

$$@\ n = 55:\ V(u) = \frac{s^2}{n}\ \frac{(N-n)}{(N-1)}$$

$$= \frac{(1.6)^2}{55}\ \frac{(309 - 55)}{(308)} \quad = 0.038$$

this would result in a standard deviation =

$$V[u]^{1/2} = (0.038)^{1/2}$$

$$= +/- .196$$

It was stated earlier that the range of the standard deviation for the single bit category is from 1.5 to 1.9, this results in a range of sample variances from 0.034 to 0.054 and standard deviations from 0.184 to 0.232.Therefore the range of the standard deviations are from 30% to about 40% and represent fairly extreme or loose tolerances. The row failure type of defect computes as follows:

$$n = 55:\quad V(u) = \frac{(.081)\ (309 - 55)}{55\ (308)} \quad = 0.0012$$

standard deviation = 0.0348

which represents +/- 87% of the mean

Problems Regarding Wafer Summary

What has begun to become apparent is that the taking of a reasonably small sample, perhaps no more than 15-20% of the population or about 45-60 sites on a wafer, is unlikely given the low frequency with which some defect categories occur. Yet to take a larger sample is undesirable given the stated goals of this project to speed up the analysis process. In addition, the tolerances being used will remain as they are in order to keep the expected error range to a minimum.

The above calculations dealt with how many sites, regardless of their analyzability, need to be sampled in order to gain an accurate estimation of the defect category proportions on each wafer. Another way to look at the problem is to determine how many analyzable sites need to be sampled. Using the single bit defect category again:

u = 1.75 single bit defects per analyzable site

$s = 1.76$

$$n = \frac{309\ (1.76)^2}{308\ (0.175)^2 + (1.76)^2}$$

$$= 76 \text{ analyzable sites}$$

Note: Again this calculation is based on a variance derived from a standard deviation equal to 10% of the mean.

Since on the average there are only 124 analyzable sites on a wafer, this would represent an average sample size of about (309/124) (76) = 190 sites which is still a lot of sites to collect information from and represents approximately 60% of the sample universe.

The conclusion then is becoming clear, in order to accurately determine the characteristics of an individual wafer such a large sample size would be required so as to preclude any benefits compared to a full examination of all sites. It would seem appropriate then to expand or alter the nature of the summary that is to be projected to consider an entire lot of wafers and all the chip sites as the sampling universe and to develop a sampling plan that could then be implemented to reproduce or estimate the lot summary. In other words, only an overall lot summary would be generated based on the sampled data that would in turn attempt to accurately predict what the last column of the existing summary would have been had it been based on a 100% count.

New Project Goal

The value to be estimated based on this new direction is the proportion of total failures for each defect type over an entire lot. That is to say, what percentage of the total failures in a lot fall under the row failure category, how many under the multiple row failure

category and so on, for all categories. In addition, the summary will be condensed to show only the estimations for each of the major categories (row failures, column failures...) rather than for each of the sub-categories. If this were to prove undesirable, the system could be easily re-expanded. When one is trying to estimate proportions the expected error (E) for the estimated proportions can be calculated as follows:

$$E = t_a [(p(1-p))/n]^{1/2} \qquad \text{Eq[C]}^2$$

where t_a = "t" statistic at a = confidence level (t.95=1.96)

p = sample proportion for a given defect type

n = sample size

solving for "n" in the above equation:

$$n = p(1-p) (t_a/E)^2 \qquad \text{Eq[D]}$$

If one does not know what to expect for a sample proportion "p" then one can substitute the largest possible value for p(1-p) = 0.25 which would be worst case. Therefore, if one is interested in limiting the error to 10% or less for the proportion estimation then one could calculate the sample size as follows:

$$n = 0.25 (1.96/0.1)^2$$

$$= 96 \text{ analyzable sites}$$

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2 John E. Freund, Statistics, A First Course (second edition) (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1970 and 1976) p. 262

Because the proportion of analyzable to unanalyzable sites is about 1:2 (about 1/3 of all sites are analyzable) then one should expect to sample 96(3) = 288 sites of data. By backing into the error value (E) using the sample size of 55 sites per wafer (giving 55(.33)=18 analyzable sites per wafer) over six wafers as was used for the example case:

(18 anal. sites/wafer) (6 wafers) = 108 anal. sites in lot

$$E = 1.96\ [(0.25)/(108)]^{1/2}$$

= 0.094 or less than 10% error over the entire lot.

The above analysis would be valid if all major error categories had equal likelihood of occuring on any given analyzable site but that is not necessarily the case. Therefore, using the following modified formula:

$$n = \frac{p(1-p)\ (t_a)2}{p_d\ (E)^2} \qquad \text{Eq[E]}$$

where P_d= proportion of analyzable sites that have the "d" defect

Note: This equation has been modified in order to inflate the computed value for "n" when the frequency of occurence for a given defect is very small.

Using the following values for p_d:

Values for P_d Values
Based on Past History

	Failure Type	p_d
A	Row	0.10
B	Multiple Row	0.18
C	Column	0.33
D	Multiple Column	0.13
E	Adjacent Bits	0.20
F	Single Bits	0.67

One can solve for "n" using estimated values based on past history for the value of "p" by substituting into Eq[F] as follows:

A $n = \frac{(0.04)\ (0.96)\ (1.96)^2}{(0.10)\ (0.10)^2}$ =148 analyzable or approx. (148)(3) = 444 total sites

B $n = \frac{(0.07)\ (0.93)\ (1.96)^2}{(0.18)\ (0.10)^2}$ = 139; gives 417 total

C $n = \frac{(0.15)\ (0.85)\ (1.96)^2}{(0.33)\ (0.10)^2}$ = 149; . . . 447 total

D $n = \frac{(0.05)\ (0.95)\ (1.96)^2}{(0.13)\ (0.10)^2}$ = 141; . . . 423 total

E $n = \frac{(0.08)\ (0.92)\ (1.96)^2}{(0.20)\ (0.10)^2}$ = 141; . . . 423 total

F $n = \frac{(0.57)\ (0.43)\ (1.96)^2}{(0.67)\ (0.10)^2}$ = 141; . . . 423 total

Therefore a sample size of 447 sites over an entire lot would be an appropriate sample size to take care of the worst known error category type and have an error of no more than +/- 10% at a 95% confidence level. If one wanted an overall range of 10% for the error (+/- 5%) then the worst case sample size would be:

$$n = \frac{(0.15)(0.85)(1.96)^2}{(0.33)(0.05)^2}$$

n = 594 analyzable or 1781 total sites

Using the pre-selected sample size of 55 sites per wafer and Eq[D] the error for the worst case (column failures) can be computed as follows:

$$E = 1.96\left[\frac{(0.15)\ (0.85)}{(0.33)(55)(0.33)}\right]^{1/2}$$

= 28.5% error

Note: One of the "0.33" factors in the denominator refers to the P_d value while the other is the 2:1 factor for inflating the sample size to account for unanalyzable sites.

Sample Size Conclusion

In conclusion, the recommended sample size over an entire lot should be about 450 sites for an error range of no more than +/- 10% at 95% confidence. The number of sites per wafer would vary depending on the lot size. A small lot might have 10 wafers in it; a large one could have up to 25. Therefore, the per-wafer sample size would range from 450/25 = 18 to 450/10 = 45.

This concludes the selection of the sample size to be used. It was necessary to start this analysis with the sample size determination for it resulted in a change in direction for the project. The initial intent was to be able to reproduce a wafer summary based on a sample. This has proven to be inappropriate given the low frequency of defect occurrence for some failure categories. The next section will deal with some of the concerns regarding the error that can be inherent in a sample based estimate and then several sampling methods will be examined. Adjustments to the sample size criteria would have to be modified as more and more live data is collected. Since the detected p and p_d factors will change with time, so too will the required sample size.

SAMPLING ERROR

In any statistical sampling situation thought must be given to the accuracy and precision of the method in use. Accuracy is the degree to which an estimate approximates the true desired value for the universe under study. Precision refers to how well an estimate based on a sample compares to a 100% count of the universe.

For the current laser host system all summaries that have been produced to date have been based on 100% counts over selected wafers. The accuracy of the 100% counts has not been determined, instead it has been considered acceptable if for no other reason than it is the only method of laser repair failure mode analysis available. The purpose of this study is not to determine the present system's accuracy, but instead to select a means of improving the system's performance by speeding it up and measuring the precision of the newer, faster method over the old 100% counting method.

In many sampling applications error is introduced into a study by the collection process itself. Therefore, a 100% counting of data

could actually have more inaccurate results than those based on a sample. In this application, one can assume that the computer method of data collection and error pattern recognition is consistent regardless of the amount of data involved. Therefore, it is not considered likely that a sample based estimate could be more accurate than a result based on a 100% count. The goal is to minimize the deviation of a sampled estimate from one based on a 100% count.

In addition to sampling error there are three other areas where error is often introduced.

1. Reporting and processing errors
2. Error due to sample plan bias
3. Sampling selection errors

Given the amount of data one is able to collect and analyze with modern computer equipment it is very difficult to both discover and trace the source of reporting and processing error. For this laser repair application, the assumption will be made that the present computer output represents a reasonably accurate account for a 100% sampling of the data.

Bias errors refer to assumptions made about a universe of data that may be unjustified. For example, as will be seen later when the

stratified sampling method is discussed in detail, the sites on the wafer can be broken down into six (6) logical segments known as radial zones. It is currently believed that each of these zones should display different yield characteristics. A "belief" that this is the most appropriate break-down is not conclusive, indeed maybe a north-south-east-west breakdown of the sites is more appropriate. Therefore, a judgement error may have been introduced that will produce a biased result.

Finally, the third type of error to be cognizant of is sampling error. Even if one is very careful in selecting and executing a sampling technique it is still possible to have, on occasion, selected a group of sites which are not proportionately representative of the universe. This can be caused by a poor random number generator that does not generate truly random number sequences or it can even be caused by, in this examle, system software problems that can occur at many different points in the data collection and analysis process.

In a system of this size one must design as carefully as possible to be wary of all sources of error infiltration. In addition, "sanity" checks should be performed periodically to measure system accuracy perhaps by running the old 100% count based system and the new sample based one in parallel. To discover discrepancies and perhaps make adjustments to the sampling strategies.

THE SAMPLING METHOD

The next decision to be made regarding a sampling strategy is the method of taking the sample. There are many sampling methods to choose from. Among the many tradeoffs to be considered are accuracy, ease of implementation and applicability. The following four sampling methods were considered for this project:

1. Random
2. Stratified
3. Systematic
4. Sequential

In order to be able to compare the various sampling plans a number of different parameters were calculated for each plan including the 100% count. The goal of course is to take a sample whose

characteristics are similar to the 100% count. The fields that are calculated for comparisons are as follows:

1. Mean
2. Standard deviation
3. Standard error of the mean
4. Conversion to standard units (z)
5. Upper and lower boundary limits

When these values were calculated for the six wafers comprising the test universe (Appendix A) the results for the single bit category were as follows:

n = 672 analyzable sites

Sumx = 1142

$Sumx^2$ = 4008

u = mean = 1.699

s = standard deviation = 1.755

Therefore one would like a sample plan whose parameters closely resemble these statistics 100% count. In all the tests of the various sample plans the single bit failure category was used for the test. In order to be more thorough in the method analysis all failure categories should have been tested. In the interest of keeping this study on a reasonable time schedule the other categories were not examined.

Random Sampling

In the sampling application at hand random sampling can be employed by using a random number generator and selecting "n" sites for analysis over a universe comprising all the sites in a lot. This procedure assumes that all sites on all wafers, regardless of physical location, have an equal probability of incurring any given failure type. This may not be a reasonable assumption since some error types are suspected of having a high geographical dependency. The stratified sampling method should be more sensitive to this condition then random sampling.

The random sample (Appendix C) was taken from the example wafer maps that are being used throughout this study (Appendix B). A random number table was used to determine the sample by assigning a sequential numbering scheme to the chip sites (i.e. 0 - 308) and using the first three digits of the random numbers. The sampling was conducted until fifty five (55) different sites were identified. This sample size of fifty five, as mentioned earlier, was used because all the analyses that were conducted in the early stages of this project were based on the understanding that fifty-five sites would be an appropriate sample size. As it has turned out, on the lot size of six wafers which are being used for all the examples a sample size of 450/6 = 75 would have

been more appropriate. Appendix C shows the failure count at each sampled site and whether or not the site was analyzable (a "-" means the site was unanalyzable). It is important to note that any site that had not already been selected was eligible for sampling (sampling without replacement); it did not have to be an analyzable site. Therefore, the number of sites with data will differ for each wafer sample. Another approach might be to randomly select site information until 55 sites with data have been chosen but on some low yielding wafers this could require a near 100% examination of the wafer and may defeat the purpose of trying to sample.

In the interest of keeping the data link running at full speed it is preferred not to analyze the data as it is being transmitted. The preference is to establish all desired sites for data collection before any transmission begins and let the laser host micro-computer send only those from which information is desired. The choices for data collection procedures will be discussed in the final conclusions.

By examining the data that was collected one can determine the following:

n = total number of analyzable sites = 101

$Sumx$ = total number of defects = 162

$Sumx^2$ = 555

u = average number of errors per analyzable site = 1.6

$$s^2 = \text{variance} = \frac{n(\text{Sum}x^2) - (\text{Sum}x)^2}{n(n-1)}$$

$$= \frac{101(555) - (162)^2}{101(100)}$$

$$= 2.95$$

$$s = \text{standard deviation} = (2.95)^{1/2} = 1.718$$

$$s_u = \text{standard error of the mean}^3 = \frac{s}{(n)^{1/2}}$$

$$= \frac{1.718}{(101)^{1/2}}$$

$$= 0.171$$

$$m = \text{population mean} = \frac{\text{total single bit errors}}{\text{total anal. sites}} = \frac{1142}{672}$$

$$= 1.699$$

---

[3]Chris Spatz and James O. Johnston, Basic Statistics, Tales of Distributions (Brooks/Cole Publishing Company, Monterey, California, 1976 and 1981) p. 154

converting to standard units:[4]

$$z = \frac{u - m}{S_u} = \frac{1.604 - 1.699}{0.171} = -0.556$$

The corresponding area under the normal curve for z = 0.556 is .2123. Subtracting from .5000 one obtains .2877 as the area below u = 1.604. Therefore the probability is roughly 29 out of 100 that the mean of a random sample with n = 101 will be less than 1.604.

To look at the error limits bounding this situation (at 95%) one performs the following:[5]

LL = lower limit = u -(1.96)(su)

= 1.604 - [(1.96) (0.171)]

= 1.27

UL = upper limit = u +(1.96)(s_u)

= 1.94

---

[4]John E. Freund, Statistics, A First Course (second edition) Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1970 and 1976) p. 157

[5]Sidney J. Armore, Introduction to Statistical Analysis and Indifference (John Wiley & Sons, Inc., New York, 1966) p. 457

If one studies the sampled data in Appendix C one notices a large number of sampled sites that provided no defect information because they were unanalyzable. The site designations are in the form of the x, y coordinates of the wafer (see wafer map examples in Appendix B).

Wafer number 42 appeared to have a significantly lower number of analyzable sites in the sample (6) compared to the others (ranging from 13 to 24). As a test to see what the effect would be on the sampling plan's calculated values, wafer 42 was omitted:

$n = 95$

$Sum_x = 156$

$Sumx^2 = 529$

$$s^2 = \frac{95\ (529) - (156)^2}{95(94)} = 2.902$$

$s = 1.704$

$$s_u = \frac{1.704}{(95)^{1/2}} = 0.175$$

One can compare these new values with those from before and see how they measure up to the 100% count:

Mean and Standard Deviation Values for Samples With and Without Wafer 42

	With		Without	
	$\bar{u}$	$\bar{s}$	$\bar{u}$	$\bar{s}$
100% sample	1.699	1.755	1.731	1.791
% Delta	-5.6	-2.1	-5.1	-4.9
Random sample	1.604	1.718	1.642	1.704

Therefore, based on this demonstration, one can conclude that the extreme nature of wafer 42 does not seem to adversely effect the sampling plan. The differences between the means of the sample and the 100% count did not change appreciably, therefore a change in procedure based on wafer characteristics is not warranted. All sampling plans were measured based on both the inclusion and exclusion of wafer 42 to check for any severe variations. One could perform all sampling plans with and without each wafer to see if any particular type had an overwhelming effect on any given sampling plan. This was decided against because there is no guarantee that the six example wafers represent all types of sampling populations that may be encountered. In fact it is almost certain that more extreme wafer types would be sampled in a continuous operations environment; therefore, any further

studies conducted to detect individual wafer impact would be inconclusive.

From the standpoint of implementation ease random sampling would be relatively simple. It would require the existence of a random number generator in the system from which to determine the sites to be sampled. The handshake process between the host system and the laser testing equipment could be one of having the tester transmit the site number and have the host make a decision regarding transmission. Two other approaches could be to have all site data sent over the link and discarded at the host end or have the laser micro-computer loaded with which sites to sample. An examination of the impact at both ends for each type of handshake would need to take place before final implementation. All the host system would have to know prior to starting the analysis of a lot is how many wafers are present so that it can run the random number generator before each wafer is tested and determine the appropriate sites to sample before testing begins.

Radial Zone Stratified Sampling

In cases where one knows that sampled data can be biased depending on where or how it is collected and can also qualify the nature of the bias, it would be appropriate to employ some form of

stratified sampling technique. A stratified sample should reflect some known characteristic of the population. In the case at hand it is a suspected characteristic that certain zones (or areas) of a wafer will demonstrate error signatures that differ significantly from the other areas.

The present accepted manner of logically breaking down a wafer into zones is to break the wafer down into six (6) radial zones (Figure 1). The center zone has only ten (10) sites associated with it and would be analagous to the "bulls-eye" on a dart board. The next zone or ring of sites would form a border around but would not include the first zone. This continues until one reaches the edge of the wafer where zone six (6) comprises only those sites that form the outer edge, approximately one to two sites deep, around the wafer and encompasses 98 chip sites.

In this study the number of sites randomly selected from each zone was based on the ratio of sites in the zone to the total number of sites on the wafer. For example, zone six has 98 sites associated with it, therefore the number of sites to sample would be [(98)/(309)](55) = 17. Therefore, the breakdown is as follows:

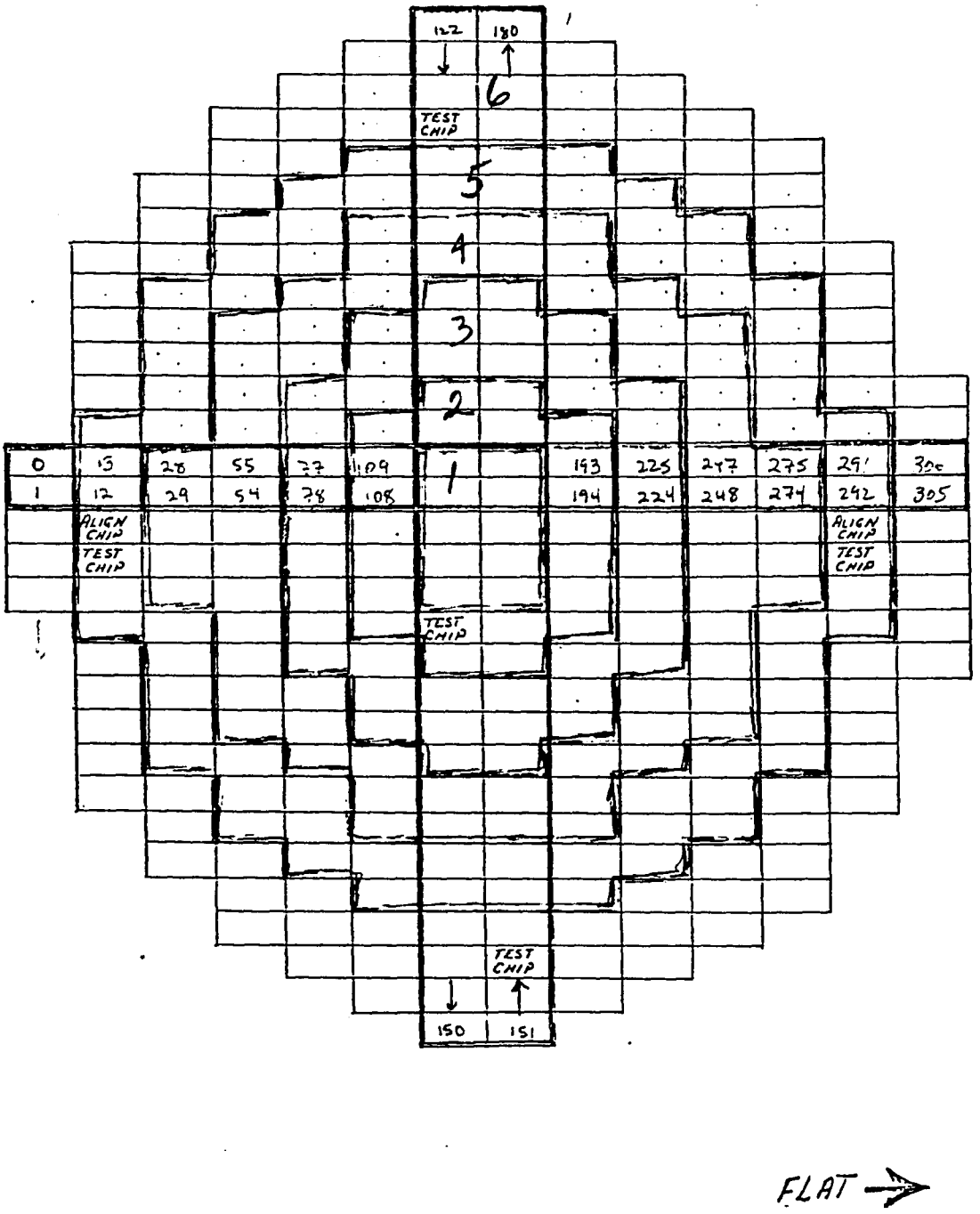

Figure 1
Wafer Map Showing
The Six Radial Zones

Sample Distributions for
Radial Stratification of a Wafer

Zone	Number of Sites	Number to Sample
1	10	2
2	21	4
3	42	7
4	68	12
5	70	13
6	98	17
Total	309	55

The sampled data should then be evenly (or proportionately) collected over all the radial zones and should help to discount the effect of each zone's unique characteristics. The same random number table was used in this instance as in the random sample application. This time, though, as a site was selected the zone count it was associated with was incremented in order to keep track of how many sites were sampled from each zone. If a site was selected that would cause the counter for its zone to exceed the pre-determined limit then it was discarded and another selection was made. This continued until 55 sites were sampled that satisfied the stated guidelines.

An interesting observation was made towards the end of this exercise. As many of the zone counters reached their limits, more and more sampled sites were discarded in order to try and sample the few

that were required to complete the other zone samples. The impression felt was one of forcing the samples to fit a prespecified format that may be biased. The results, when compared to the other sample plans, tend to support this observation for this plan resulted in the worst sample from the standpoint of duplicating the known lot characteristics. On the other hand, the biased nature of the results do suggest that the six radial zones and their sample results may provide other unexpected information that will be discussed further in the "results analysis" section. The statistics generated from the same set of wafer data as that used for the random sample is as follows (see Appendix D for the data):

$$n = 112$$

$$\text{Sum}x = 166$$

$$\text{Sum}x^2 = 578$$

$$s^2 = \frac{112(578) - (166)^2}{112(111)} = 2.991$$

$$s = 1.729$$

$$u = 1.482$$

$$s_u = \frac{1.729}{(112)^{1/2}} = 0.163$$

$$z = \frac{u - m}{s_u} = \frac{1.482 - 1.699}{0.163} = -1.328$$

$$UL = 1.482 + 1.96\ (0.163) = 1.801$$

$$LL = 1.482 - 1.96\ (0.163) = 1.163$$

One aspect of the proposed stratified sampling plan that may inject some unwanted bias into any estimate calculations is the fact that each zone is a different size. In traditional stratified sampling one would normally try and set up the stratification such that the population of each strata properly represents the specific characteristic that one is trying to isolate in addition to keeping the sizes of the various stratas the same whenever possible.

Quadrant Zone Stratified Sampling

As was mentioned earlier, it is only an educated guess that provided the six zone stratification of the wafer. This may not be appropriate perhaps a north-south-east-west orientation of quadrants would be more sensitive to the bias being isolated. The same data that was examined for the previous two sampling plans was used only this time the wafers were logically broken up into quadrants of approximately equal size (see Appendix E). Within each quadrant of each wafer sites were selected "systematically", for this method of sampling is easier to perform when taking a manual sample. A random number between one and six was generated and determined the starting site for any given quadrant of any given wafer. After that every sixth site was selected for inclusion in the analysis. This was done for each quadrant on each of the six sample wafers to make up the total sample

population. If this were to be the method chosen for the final application a random sample within each quadrant would be more appropriate. With the systematic sampling approach it is always possible that one might, by chance, come across a defect pattern which occurs with the same systematic consistency as the sampling plan. A random sample would help minimize the danger of this happening.

The results for this variation of stratified sampling over the six sample wafers are as follows (see Appendix F for data):

Results for Quadrant Stratification

Zone	Sumx	$Sumx^2$	n	u	s	s_u	z
1	39	125	27	1.44	1.63	.31	- .81
2	34	102	26	1.31	1.52	.30	-1.27
3	69	249	33	2.09	1.81	.32	1.25
4	37	111	29	1.28	1.51	.28	-1.46

Grouped together as one large sample, the results are as follows:

$n = 115$

$Sumx = 179$

$Sumx^2 = 587$

$$s^2 = \frac{115\ (587) - (179)^2}{115(114)} = 2.705$$

$$s = 1.645$$

$$u = 1.557$$

$$s_u = \frac{1.645}{(115)^{1/2}} = 0.153$$

$$z = \frac{u - m}{s_u} = \frac{1.557 - 1.699}{.153} = -.928$$

$$UL = 1.557 + 1.96\ (.153) = 1.857$$

$$LL = 1.557 - 1.96\ (.153) = 1.257$$

If one studies the results for the individual zones one will notice an apparent difference between the zones. A discussion regarding these differences will follow in the "results analysis" section.

The results demonstrated by the use of quadrant zones compare favorably with those obtained through the random sample. When the four individual quadrant results were combined the resultant sample mean differed from the population mean by only 8.4% on the low side. There will be a further discussion of this plan later in this report.

From a system implementation point of view the software development required for either form of stratified sampling would be about the same and would be more involved than the simple random

sampling plan. The system should probably be set up to generate the randomly selected sites for each zone at the beginning of a wafer test and supply that list of sites to the laser repair micro-computer. What is important is that the number of sites chosen for each zone be kept straight so that the proper spread and stratification is maintained.

Interpenetrating Replicate Subsamples

Another form of stratified sampling is "interpenetrating replicate subsamples." This scheme is good for obtaining quick estimates for preliminary results. What one does is randomly break down a universe into smaller and smaller samples at which point each of the lowest-level samples are themselves sampled. If one thinks of the universe as all the chips in a lot then each wafer could be considered a sample of the lot and a sampling of sites on each wafer would be a further sub-sample. But since the population of sites on a wafer is not random, they are fixed within a wafer, this would not be a sensible application of this method. If one could view all the chip sites in a lot as the population and would be able to subdivide that entire population several times in a random manner, this form of stratified sampling could then be considered. In other words, if the population was identified as the following:

Wafer, Chip Site
01 000
01 001
01 002
.
.
.
25 308

The population would then comprise 25 x 309 = 7725 chip sites in a 25 wafer lot and an appropriate scheme for employing interpenetrating replicate subsampling could be employed.

What one could do is take a number of large samples perhaps ten samples of fifty chip sites, and then maybe two or three out of those ten samples for analysis. Due to the scope of manually performing this type of application it was not exercised for this study. It would provide a quick estimate of the characteristics of a lot but would require rather sophisticated software development.

Systematic Sampling

Systematic sampling techniques were the next plan considered for this project. In systematic sampling one determines a fixed selection

pattern for the collection of data. For example, randomly select a number 'i' between 1 and 5, start with that site number and select every other site thereafter over any given wafer. This is also known as patterned, serial or chained sampling.

For the execution of this sampling plan a per wafer sample size of 61 will be used to apply the systematic sampling technique. Randomly selecting a number between one and five using a random number table yielded the value 5, therefore starting with site number five on the first wafer and selecting every fifth value thereafter the following sample statistics were collected (see Appendix G for the data):

$$n = 146$$

$$Sumx = 222$$

$$Sumx^2 = 752$$

$$u = 1.521$$

$$s = 1.691$$

$$s_u = \frac{s}{(n)^{1/2}} = \frac{1.691}{(146)^{1/2}} = 0.140$$

$$z = \frac{u - m}{s_u} = \frac{1.521 - 1.699}{0.140} = -1.271$$

where m = population mean

Looking at the error limits:

$$LL = u - 1.96\, s_u$$
$$= 1.521 - 1.96(0.140) = 1.247$$

$$UL = u + 1.96\, s_u$$
$$= 1.521 + 1.96(0.140) = 1.795$$

As mentioned earlier, the danger of using systematic sampling is that the system chosen may have a strong correlation to a systematic failure pattern on the wafer. If so, the results could be heavily skewed one way or the other. The results from this sampling plan proved disappointing by comparison to the others although it did provide a slightly better sample than the stratified sampling plan that was based on radial zones. From a software development standpoint systematic sampling would be quite straightforward. The use of the random number generator could determine the starting point and a sequential sampling of the sites would provide the sample.

Comparing the Sample Plans

The calculated results from each of the sampling plans are summarized in Table 1. The first item in the table, the 100% count

TABLE 1

SAMPLING PLAN COMPARISONS

	1	2	3	4	5	6	7	8	9	10	11	12
	n	Sumx	$Sumx^2$	u	%	$\bar{5}$	%	s_u	z	UL	LL	Range
100% Count	672	1142	4008	1.699	NA	1.755	NA	NA	NA	NA	NA	NA
Random	101	162	555	1.604	- 5.6	1.718	-2.1	0.171	-0.556	1.939	1.269	0.670
Stratified (radial zones)	112	116	578	1.482	-12.8	1.729	-1.5	0.163	-1.328	1.801	1.163	0.638
Stratified (quadrants)	115	179	587	1.557	- 8.4	1.645	-6.3	0.153	- .928	1.857	1.257	0.600
Systematic	146	222	752	1.521	-10.5	1.691	-3.6	0.140	-1.271	1.795	1.247	0.548
Without Wfr 42												
100% Sample	617	1068	3708	1.731	NA	1.791	NA	NA				
Random	95	156	529	1.642	-5.1	1.704	-4.9	.175				
Stratified (radial)	105	159	551	1.514	-12.5	1.73	-3.4	.169				
Stratified (quadrants)	106	167	557	1.575	- 9.0	1.67	-6.8	.162				
Systematic	134	207	673	1.545	-10.7	1.63	-9.0	.141				

refers to the current system approach where no sampling is performed. Column four shows the mean for each sample type and column five shows the difference between each plan and the 100% sample. The pure random sample returned the best results in terms of the differences between means where the sampled mean was only off by 5.6 percent. The differences between the sampled and the true standard deviation are shown in column seven.

Earlier in this report wafer 42 was cited as appearing to be significantly different from the other five wafers in our example. For the sake of seeing if the general results of this study are skewed by the existence of this unusual wafer each of the sample plans were conducted with and without wafer 42. The results excluding this wafer are shown in the bottom half of Table 1.

The stratified sampling plan using the six radial zones had the smallest difference between standard deviations. The radial zones that were chosen may be forcing a bias that is giving the least deviation from the sampled mean but is not necessarily providing a good estimate of the population mean. In other words, the radial zone application provides for a fairly homogeneous sample although it appears to compare to the true population characteristics very poorly.

Analysis of Variance

In an effort to help strengthen the choice of a sampling plan an analysis of variance (ANOVA) was performed on the various sampling plan results. The set of calculations performed are demonstrated as follows:[6]

	100% Count	Random Sample
n	672	101
Sumx	1142	162
$Sumx^2$	4008	555

$T = Sumx_a + Sumx_b$

where $Sumx_a$ denotes total sum of the x's for sample type "a"

$$C = \frac{T^2}{(n_a + n_b)} = \text{correction term}$$

SST = sum of squares for the total

$$= \text{Sum}\,[(x_{ai},\ i=1,\ \ldots,n_a)^2+(x_{bi},\ i=1,\ \ldots,n_b)^2]-C$$

SS(TR) = sum of squares for the sample plans

$$= \frac{(Sumx_a)^2}{n_a} + \frac{(Sumx_b)^2}{n_b} - C$$

SSE = sum of squares for the error (residual)

$$= SST - SS(TR)$$

---

[6]Irwin Miller and John E. Freund, Probability and Statistics for Engineers (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1977) p. 339

Therefore the calculations comparing the 100% count to the random sample calculation are as follows:

$$T = 1142 + 162 = 1304$$

$$C = \frac{(1304)^2}{(672 + 101)} = 2199.8$$

$$SST = (4008) + (555) - (2199.8) = 2363.2$$

$$SS(TR) = \frac{(1142)^2}{672} + \frac{(162)^2}{101} - (2199.8) = 0.8$$

$$SSE = 2363.2 - 0.8 = 2362.4$$

ANOVA TABLE (Random vs. 100% Count)

Source	ss	df	ms	F	$F_{0.05}$
Sample plans	0.8	1	0.8	0.3	3.84
Error	2362.4	771	3.1		
Total	2363.2	772			

The one degree of freedom for the sample plan source comes from the fact that only the two sample plans have been combined for the purposes of analyzing the variances. The number of degrees of freedom for the total comes from the fact that there were 773 pieces of data between the two sample plans.

Therefore it can be concluded that since the calculated F statistic of 0.3 is less than the critical F at the 0.05 level the hypothesis that the random sampling plan is providing a mean estimate that is consistent with the 100% count cannot be rejected. If the calcualted F had exceeded $F_{0.05}$ then one would have to assume that the sampling plan is introducing a bias that will have a significant effect on the sample based results.

The results of the ANOVA's that were performed comparing each sample plan to the actual are summarized in Table 2. As the calculated F statistic approaches zero the mean and variance of the sample approach those of the actual. The F statistic for random sampling had the lowest value at 0.3 where the critical $F_{0.05}$ equals 3.84. This suggests that a very good sample was taken compared to the stratified sampling plan that followed the radial zone stratification which provided an F statistic of 13.2. The fact that the radial stratification resulted in such a large F statistic indicates that the

TABLE 2

ANOVA OF EACH SAMPLING PLAN

COMPARE EACH METHOD TO 100% COUNT

		SS	df	MS	F	$F_{0.05}$	Sig?	N	Sumx	$Sumx^2$	C
		0.8	1	0.8	0.3	3.84	N	773	1304	4563	2199
Random	Err	2362.4	771	3.1							
	Tot	2363.2	772								
		42.3	1	42.3	13.2	3.84	Y	784	1258	4586	2018.6
Strat	Err	2525.1	782	3.2							
(radial)	Tot	2567.4	783								
		2.0	1	2.0	.67	3.84	N	787	1321	4595	2217.3
Strat	Err	2375.7	785	3.0							
(quad.)	Tot	2377.7	786								
		3.9	1	3.9	1.3	3.84	N	818	1364	4760	2274.4
Syst.	Err	2481.7	816	3.0							
	Tot	2485.6	817								

six radial zones forced a sample with a single bit defect category distribution that is quite different from the population it was taken from. Although this ANOVA study has helped negate the use of radial stratification as a sampling method, at least in the suggested form, it has highlighted an area that deserves further investigation. In other words, the variation in the mean of the 100% count compared to the radial stratification example are due to something more than error and expected variations.

Sample Plan Conclusion

Based on the results of the ANOVA for the sampling plans random sampling and stratified sampling using quadrant stratification gave the two best performances. This stratified sampling plan will be examined further in the "results analysis" section and will show that more information is made available from this plan compared to the random sample without significant loss in sampling quality.

The recommended sampling plan is to take a sample of 450 chip sites from a lot regardless of their analyzability, evenly distributed over each wafer, and to take a stratified sample within each wafer. The wafer samples should be broken up into four x-y quadrants (or stratas) and an even number of randomly sampled sites chosen from each.

The results should then be presented for each quadrant over the entire lot and also an analysis performed to determine the overall lot characteristics. The next section, results analysis, will illustrate and discuss how the information could be presented.

RESULTS ANALYSIS

The lot summary report in its present form (Appendix A) provides a great deal of information in a reasonably concise package but does little to point the user of the report in a direction for action. The report presently provides all the appropriate data counts for the failure categories and how each one compares with any other in terms of the percentage of total failures (upper half) or percentage of sites that show each failure type (lower half). What is most important to the user is determining what failure type seems to have the greatest correlation to the yield fluctuation. This information would be useful because each failure category can point an educated product engineer to a particular step in the manufacturing process for corrective action. If this can be done reliably and quickly then action can be directed at the specific manufacturing problem and one can avoid tieing up precious resources trying to analyze an entire manufacturing line. Perhaps the ultimate goal should be to develop a system that automatically collects and analyzes the data and determines exactly what corrective action should be taken to improve the yields. This study will only deal with

elevating the sophistication of the output so as to point out the relative significance of each failure category; the human interface will still have to translate that information into a sensible action plan.

Proposed Lot Summary

In part one of this paper a sampling scheme was developed that would help cut down the amount of data that has to be analyzed to present a reasonably accurate account of a lot's error signatures. With the sampling plan successfully implemented, one would be able to collect data from virtually all the lots that pass through the laser repair facilities. It is therefore easy to imagine a situation where a large amount of data could be assembled representing summaries of samples taken from each wafer in each lot that passed through the area. It would largely be only data and is not necessarily very informative to the user. Apendix "H" shows an example lot summary for ten lots from number 5084 to number 5095. Although this particular summary is ficticious it is not impossible to imagine that this could represent one day's worth of data.

The user of this report would be able to tell, for example, that there were about 120 detectable failures per wafer on lot 5084 and there was a failure rate of about 2.18 failures per analyzable chip and

an approximate yield of about 64 chips per wafer. In addition, the user knows that the single bit defect category occured with the greatest frequency; 62% of the defects sampled were of the single bit variety. What the user does not know is whether or not this failure type has the greatest correlation to the yield fluctuation. A single bit defect by itself is pretty easy to repair and if there aren't too many of them scattered far apart it may have little impact on the yield because a repaired chip is considered as good as a virgin chip (a virgin chip is one that demonstrates no failures of any kind). It would therefore be useful to present some information regarding the correlation of each failure type to the measured yield.

Failure Correlation to Yield

The correlation co-efficient was calculated for each major defect category both for the "percentage of total defects" and "percentage of total analyzable sites" portions of the report. The calcuations used were as follows:

Terminology [7]

x_i = percentage of row railures for lot "i"

y_i = yield for lot "i"

n = number of lots (10)

[7] Irwin Miller, John E. Freund, Probability and Statistics for Engineers (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1977) p.323

$Sumx = Sum\ x_i\ (i = 1, \ldots, n)$

$Sumx^2 = Sum\ x_i^2\ (i = 1, \ldots, n)$

$Sumy = Sum\ y_i\ (i = 1, \ldots, n)$

$Sumy_i^2 = Sumy_i^2\ (i = 1, \ldots, n)$

$Sumxy = Sumx_iy_i\ (i = 1, \ldots, n)$

$Sxx = n(Sumx^2) - (Sumx)^2$

$Syy = n(Sumy^2) - (Sumy)^2$

$Sxy = n(Sumxy) - [(Sumx)\ (Sumy)]$

r = correlation coefficient = $(Sxy)/[(S_{xx})\ (S_{yy})]1/2$

r^2 = percent of variation attributable to given defect

Calculation for Defect Type A

Data for Defect Type A (% of Total Defects)

	Lot	1	2	3	4	5	6	7	8	9	10
	Yield	64	103	98	118	137	136	97	126	152	196
A.	Row Failures	7	3	2	2	5	6	1	5	1	1

$Sumx = 33$

$Sumx^2 = 155$

$Sumy = 1227$

$Sumy^2 = 162303$

$Sumxy = 3765$

$S_{xx} = 10(155) - (33)^2 = 461$

$S_{yy} = 10(162303) - (1227)^2 = 117501$

$S_{xy} = 10(3765) - [(33)\ (1227)] = -2841$

$r = (-2841)/[(461)\ (117501)]^{1/2} = -.386$

$r^2 = .149$

Note: Table 3 shows the correlation for all the defect categories for the top half of Appendix H (the lot summary).

The calculations for the bottom half of the lot summary are essentially the same and are detailed in Table 4. What differs between the top and bottom halves of the report in Appendix H is the interpretation. When one is reading the top half the percentage values refer to percent of total defects. That is to say, 62 percent of all defects found on lot 5084 were categorized as single bit defects and they occured on 47 percent of the sites (bottom half). The subtle differences between the two halves are that any given defect that is counted is categorized into one and only one category whereas any given

site can be associated with any number of different defect types. Therefore the percentages in any given column in the top half add up to 100 whereas the percentages in the bottom half have no finite limit.

Interpretation of Lot Summary

Referring to the last two columns on the right hand side of the summary one will notice that row failures for category A, had the highest correlation (-.386) and it is negative suggesting that as the number of row failures increase the yield goes down. This is interesting for one would expect an inverse relationship between yield and the number of errors found. Only categories A and F exhibit this inverse relationship while all others are positive albeit with a relatively small magnitude. Although the volume of defects and yield are expected to have an inverse correlation one should not have any preconceived notions about what the relationshp between defect ratios and yield should be. If the correlation coefficient were of sufficient magnitude to be considered significant and was greater than zero, a fascinating phenomenon would exist that, when explained, could have a major impact on yield management.

A positive correlation would indicate that as the ratio of defects for the given category increases, the yield shows a

TABLE 3

CORRELATION OF DEFECT FREQUENCIES TO YIELD

	1	2	3	4	5	6	7	8	9	10	Sumx	$Sumx^2$	Sumxy	Sxx	Sxy	r	r^2
A	7	3	2	2	5	6	1	5	1	1	33	155	3765	461	-2841	-.386	.149
B	10	6	3	4	13	9	3	4	4	8	64	516	8000	1064	1472	.132	.017
C	11	22	17	16	9	12	1	22	12	14	136	2200	16826	3504	1388	.068	.005
D	2	9	3	4	3	5	1	6	2	2	37	189	4461	521	- 789	.101	.010
E	5	10	5	5	9	13	3	4	5	6	65	511	8162	885	1865	.183	.033
F	62	46	67	67	54	50	91	54	71	67	629	41081	76931	15169	-2473	-.059	.003
G	2	3	2	1	4	4	0	1	3	1	21	61	2621	169	443	.099	.010
H	1	1	1	1	3	1	0	4	2	1	15	35	1934	125	935	.244	.060
Yield	64	103	98	118	137	136	97	126	152	196	1227	162303		117501			

TABLE 4

CORRELATION BETWEEN SITES W/DEFECT AND YIELD

	1	2	3	4	5	6	7	8	9	10	Sumx	$Sumx^2$	Sumxy	Sxx	Sxy	r	r^2
Row Fail.	13	9	6	7	12	11	8	10	2	3	81	777	9241	1209	- 6977	-.585	.343
Mul. R.F.	20	16	11	12	26	19	15	11	10	3	143	2413	16517	3681	-10291	-.495	.245
Col. Fail.	14	54	54	31	20	23	8	40	27	26	298	11016	36356	21356	- 2086	-.042	.002
Mul. C.F.	4	25	13	13	8	10	4	13	5	5	100	1378	11861	3780	- 4090	-.194	.038
Adj. Bits	11	27	16	13	21	24	12	10	13	12	159	2849	19480	3209	- 293	-.015	.0002
Sngl. Bits	47	68	90	83	59	56	100	65	71	60	699	51305	84767	24449	-10003	-.187	.035
Unrecog.	4	11	8	5	10	8	0	3	6	2	57	439	6903	1141	- 909	-.079	.006
Too complex	54	35	44	43	10	24	87	18	31	18	364	17780	40028	45304	-46348	-.635	.404
PRE. SCREEN	1	1	2	1	1	2	1	1	0	0	10	14	1113	40	- 1140	-.526	.277
Yield	64	103	98	118	137	136	97	126	152	196	1227	162303		117501			1.073

proportionate increase. There would have to be some extensive investigation conducted to explain such a relationship and to determine when one reaches the point of diminishing return. It is not impossible to imagine that when a particular failure category reaches 100% of all defects observed the yield is maximized for it may be an easily repairable defect type that does not have a detrimental effect on yield.

The lower half of the report shows the correlation co-efficient as measured between the percent of sites exhibiting any given defect and this time all the "r's" are negative. Again this is expected for as the number of defects increase on a given site the ability to repair decreases thus leading to this inverse relationship. Once this system is in place, it would be interesting to see if any of these relationships turn positive and to try and explain such a condition.

The "too complex" category showed the greatest correlation to yield at -.635 and 40.4 percent of the variation. This is not surprising since the definition of a too-complex chip site is that it has more defect types than can be reliably determined therefore it is discarded for analysis and considered unanalyzable. If a chip site has so many different errors that it can not be analyzed by the system's software it probably cannot be repaired, thus decreasing the yield. The

second greatest correlation is, as before, the row-failure category at -.585 and 34.4 percent of the variation. If this were an actual summary, representing real data an appropriate first step for the product engineer to take would be to determine what the primary cause of a row failure is, at what process step does the problem occur, and what is the appropriate process parameter to change. This system output would also provide the user with some indication as to how big an impact a proven change that is known to effect row failures would have on the yield. Since a direct relationship between yield improvement and cost reduction can be established by way of this summary the amount of effort required for a process change can be justified depending on its financial impact.

In addition to the above correlation, another one was performed comparing all defect types to each other. This type of analysis could be another system output that is easily generated. Table 5 shows the results of this analysis. In many cases the correlations are as expected. For example, there is a high correlation between multiple column failures and column failures. Since these failure categories are similar one would expect that as one increases so does the other. Use of this information should be to highlight unexpected correlations. For example, the high inverse relationship between single bits and multiple column failures or regular column failures would seem rather

TABLE 5
Correlation of Each Defect
To All Others

	ROW FAIL.	MUL ROW FAIL.	COL. FAIL.	MUL COL. FAIL.	ADJ. BITS	SINGLE BITS	UNREC	
Mul. R.F.	.640							
Col. Fail.	.112	-.194						
Mul. C.F.	.263	-.038	.768					
Adj. Bits	.431	.577	.159	.523				
Sngl. Bits	-.630	-.497	-.678	-.773	-.727			
Unrecog.	.455	.604	.109	.313	.815	-.674		
Too Complex	.354	.192	.408	.372	-.015	-.468	.241	
YLD	-.386	.132	.068	.101	.183	-.059	.099	.244

interesting. This is only test data and is being used for the purposes of demonstrating possible uses of the information. The true value of all these proposed reporting mechanisms comes from repeated use and careful examination over long periods of time and many sets of live data.

Detecting Changes in the Data

Once the sampling plan is in place and data over a larger set of lots is being collected, and once the summary reports are organized and presented in a manner that makes them more informative, the system is then ready to examine additional aspects of the data. One piece of information that would be interesting to the process and product engineer is knowing when a change has occured in the nature of the product. The change can be for the better or for the worse for either variation can provide important insight into the state of the product.

With the large volume of data being collected over time it would be interesting to have the system monitor and compare all the lots as they pass through the area. In other words, the system should be able to perform two primary functions:

1. Summarize each individual lot and flag any significant problems pertaining to that lot

2. Compare each lot to the series of lots that preceeded it and determine if there has been a statistically significant change in the product.

The first function has already been covered in earlier sections. The second function could be handled by comparing two samples from two different lots or series of lots and deciding whether any or all of the observed differences among the means are attributable to chance. If the differences are significant then one may be able to conclude that there is a true statistical difference between the two.

An example application of such a lot series comparison could be to compare the differences between two different oven settings at a process step. One lot series could be run through the line at the current oven settings while another would be run at the new settings. It would be vitally important to try and keep all other processing variations to a minimum in order to limit the cause of any variations in lot performance to the oven settings being tested. If one knows that the first five lots detailed in Appendix H were made under the current conditions while the second five were manufactured under the other one could perform the following using the same ANOVA procedures as outlined when comparing sampling plans:

yld_1 = mean yield for first five lots = 104

yld_2 = mean yield for second five lots = 141

h: hypothesize that both sets are from universes exhibiting equivalent means (ie. statistically insignificant differences).

Based on a simple comparison of the mean yields of the two lot series one would be tempted to claim that the new oven settings were having a significantly positive impact on the yield. The ensuing ANOVA will show that this is not necessarily the case:

Lot Series	a	b
n:	5	5
Sumx:	520	707
$Sumx^2$:	57002	105301

$T = 520 + 707 = 1227$

$$C = \frac{(1227)^2}{10} = 150552.9$$

$$SST = (57002) + (105301) - 150552.9 = 11750.1$$

$$SS(TR) = \frac{(520)^2 + (707)^2}{5} - 150552.9 = 3496.9$$

$$SSE = 11750.1 - 3496.9 = 8253.2$$

ANOVA TABLE

Source	ss	df	ms	f	f0.05
Lot Series	3496.9	1	3496.9	3.4	5.32
Error	8253.2	8	1031.7		
Total	11750.1	9			

The one degree of freedom for the lot series source of variation is due to the fact that there are only two lot series being compared ("a" and"b"). The nine degrees of freedom for the total is based on there being ten yields being examined, one per lot. Therefore one must conclude that the differences between the two means are not attributable to differences between the lot series. If the calculated F (3.4) had exceeded the critical F ratio (5.32) one would have to conclude that the difference between the means of the two sets is not entirely attributable to chance and therefore other factors must be playing a part. That other factor would most likely be the effect of the new process. As it stands now the new oven setting's apparent positive effect is not statistically significant.

An ANOVA table was set up (Appendix I) for all failure categories comparing the first five lots to the second five. It is interesting to note that the hypothesis cannot be rejected in all cases except failure types A and B where it appears there are some real differences.

All this information can start to become just as overwhelming as the original raw data was but in fact presents some very interesting information. Based on the ANOVA for the yields and defects one can hypothesize that the two different manufacturing procedures are only having a significant effect on Defect A (row failures) and B (multiple row failures). An experienced product engineer would know what process step has the greatest effect on row failure types of defects and could then try and explain why the manufacturing change is effecting that particular process step to gain greater insight into the matter. This information would serve as a means of focusing the engineer's attention to a specific area.

Analysis of Quadrant Variation

Earlier in this paper when the sampling plans were being discussed it was stated that the stratified quadrant sampling method would prove superior to simple random due to the additional information it provides. If this scheme were implemented one would be able to

compare the various quadrants to see if one is consistantly better or worse than any other. By employing the same ANOVA procedure as before one can perform the following analysis:

	Quadrant				
	1	2	3	4	Total
Mean	1.4	1.2	2.1	1.3	1.5
n	27	28	33	29	117
Sum^x 39	34	69	37	179	
$\text{Sum}x^2$ 127	102	249	111	589	

$T = 179$

$$C = \frac{(179)^2}{117} = 273.9$$

$$SST = 589 - 273.9 - 315.1$$

$$SS(TR) = \frac{(30)^2}{27} + \frac{(34)^2}{28} + \frac{(69)^2}{33} + \frac{(37)^2}{29} - 273.9$$

$$= 15.2$$

$$SSE = 315.1 - 15.2 = 299.7$$

Anova Table

Analyze Differences Among Quadrants

Source	SS	df	MS	F	F0.05
Quadrants	15.2	3	5.1	1.9	2.68
Error	299.9	113	2.7		
Total	315.1	116			

By examining these results of such an analysis one would have to conclude that the differences among each of the four quadrant means is not statistically significant. On closer examination one notices, in this example, that quadrant three appears to be much better than the others (lower right hand corner of the wafer). Another ANOVA was performed to determine if quadrant three by itself was significantly better than the others:

$T = 179$

$C = 273.9$

$SST = 315.1$

$$SS(TR) = \frac{(69)^2}{33} + \frac{(110)^2}{84} - 273.9$$

$$= 14.4$$

$SSE = 315.1 - 14.4 = 300.7$

Anova Table

Quad 3 Compared to Others

Source	SS	df	MS	F	F0.05
Quadrants	14.4	1	14.1	5.5	3.92
Error	300.7	115	2.6		
Total	315.1	116			

Therefore, when one separates quadrant three from the others its better yield does appear to be significant. Naturally one would want to observe such a situation over time to determine if this is a consistant difference or not. This analysis however helps point out the benefits made possible by this stratified sampling approach.

With all the proposed enhancements to the system the product of it all is new information for the user of the system and not just more data to sift through. A summary like the one proposed would provide a quick and dirty check of how any one lot fared as it passed through the laser repair facilities and how it compares to other lots of the same product type. If the data base was set up effectively to provide product engineering with the proper flexibility the users would be able to test many different hypotheses by comparing appropriate lot samples to each other.

Drawbacks of the Proposed System

This system would not provide all the answers but would merely present a case. One would be able to capture some information from every lot that passes through the area rather than comprehensive data collection for only those that are requested on a one-at-a-time basis. As beneficial as this proposed system would be some features of the current system would not be available unless specifically provided for. One such feature is the detection of mask failures.

In the background portion of this report the mask was described as analagous to a negative in a photographic development process. The mask is a piece of glass with a pattern made out of aluminum on the surface that maps out a specific circuit layer for its respective device design. The clarity of the image that is projected through the mask is critically important to the process. Any imperfections in the mask will tend to show up at the end of the line as recurring defects. If the same cell on the same site keeps failing a significant portion of the time, it is considered a candidate for the mask failure category. The current level of acceptance is a recurrance of 65% or more on at least six wafers. In order to discover such a situation all site information must be available; a sample would not be sufficient. This feature is considered a valuable contribution of the present laser

host system therefore it is suggested that this type of analysis remain available on the request-only basis when a comparison of two mask sets needs to be made or the close statistical examination of a single mask set is desired. It is felt that this two system availability (old and new) is a perfectly acceptable mode of operation given the benefits of the proposed system.

Another feature that could be lost with the new system is known as the bit-mapping function. A bit map is a hard copy output that shows the status of every cell on a given site. In other words, for a 64K memory device one would be able to see the status of every cell over all 65536 cells on any site of a given wafer. This would also, as in the case of the mask analysis, require a 100% sample if the user wanted to be able to examine the bit map for every site on any wafer.

There are two possible solutions to this problem. One is to have this generated on a request only basis as in the mask analysis or one could transmit all data for all sites over the data link and sample from the data residing at the host end of the data link. In other words the data would be sampled after transmission and not before as originally proposed. The advantage is the availability of all wafer data at all times but the disadvantages would include a heavy loading of the data link and storage media that could ultimately slow down the

response of the system, thus reducing the positive effects of the sampling plan. The analysis time that would be saved through sampling would not be affected by either approach.

Conclusion

The results analysis findings of this study are perhaps more important than the sampling plan portion. The correlation examination and analysis of variance could and should be performed on the currently available data regardless of the method of data collection. The insight gained into the status of any given device would prove extremely valuable and would be fairly easy to implement. The cost in terms of analysis time would be very small.

The techniques that have been discussed are only the most basic statistical tools available for use in gaining a greater understanding of a situation. Many other avenues of study need to be pursued to help unlock all the hidden information that could so easily aid the failure mode analysis cycle. Procedures should be developed to help refer the user to a specific cause of a problem rather than merely highlighting the problem itself. The thought processes of a product engineer would indeed be difficult to mechanize, but so too are those processes difficult to replace when the need arises. The more knowledge one can

define and mechanize, the more one is able to ensure a more stable FMA environment by minimizing the effect of personnel fluctuations.

The results that have been analyzed are not a true refelection of the current state of affairs; therefore any insights gained into the example data used throughout this study is of course not in itself of any great value. More ideas would almost certainly arise from a detailed analysis over many live lots. Such an analysis could perhaps unlock all sorts of mysteries or, on the other hand, it may show disappointing results from the standpoint of demonstrating anything from which to draw any conclusions. For example, the correlation coefficients calculated from real data may prove too low to be considered significant thus giving little insight into the underlying characteristics of each failure category. If so, other analysis methods would need to be pursued. Only a comprehensive live test would provide the answer to such questions.

PROJECT SUMMARY

When reflecting back upon activities that were pursued from a position of relative intellectual ignorance, one always can find decisions that could and should be changed or enhanced. The mere pursuit of the covered subject matter proved a valuable learning experience that has left this author in the position of being barely qualified to attack this project from the beginning with renewed insight into the application of data analysis techniques encompassing several areas of statistical study.

In an attempt to be sensitive to the proprietary nature of the subject matter, the in-depth analysis of real data was denied. Such analysis would undoubtedly have proved fascinating. In particular the subject of stratified sampling could be the focal point of a project by itself for it appears that there is no end of insight to be gained by examining the geographic dependencies of the various failure categories. A full blown investigation of error pattern detection could be launched by trying to determine what the proper strata or zones should be rather than making an educated guess.

More attention should have been paid throughout this study to trying to analyze the nature of the data more. The type of data distributions involved greatly affect the type of analyses that can be and should have pursued for this study. It may have been misleading to try and fit a sampling plan to the 100% count for the 100% count may be an inappropriate representation of the data. For example, when performing the quadrant strata analysis it should have been compared to a 100% count representation for each quadrant rather than the entire population.

There is no end of new analysis techniques that would have been pursued had time permitted. Completely different conclusions may have been drawn. The net result of this project was an intense learning experience for this author that has given an enhanced understanding and appreciation for the subject covering statistics and probability that will more than likely be built upon further over the years.

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APPENDICES

APPENDIX A
Original Lot Summary

ELECTRICAL FAILURE ANALYSIS - # (%) OF TOTAL FAILURES

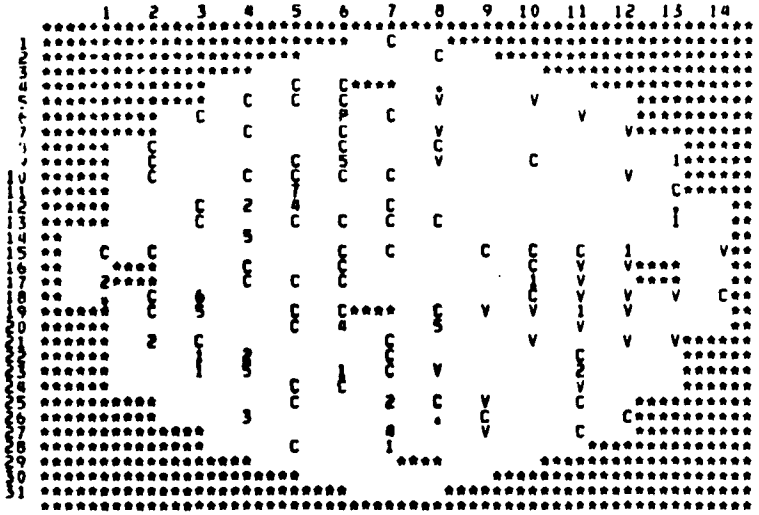
WAFER	42		02		44		37		07		05		TTL/WF	
# ANALYZABLE CHIPS	55		113		93		109		137		145		112	
# VIRGIN CHIPS	35		6		0		10		20		26		15	
# DIAG DEAD	85		53		68		46		57		46		59	
# REPAIRABLE CHIPS	44		104		109		121		131		113		106	
# FAILURES	120		373		414		360		382		341		332	
# FAILURES/ANALYZABLE CHIP	2.18		3.30		4.45		3.30		2.43		2.35		2.96	
1. ROW FAILURES	8	(7)	11	(3)	8	(2)	8	(2)	20	(5)	20	(6)	13	(4)
2. SINGLE ROWS	2	(2)	5	(1)	6	(1)	3	(1)	2	(1)	6	(2)	5	(2)
3. WEAK ROWS	2	(2)	1	(1)	1	(0)	0	(0)	1	(1)	5	(2)	2	(1)
4. ROW OPENS	3	(3)	5	(1)	1	(0)	5	(1)	17	(4)	9	(3)	6	(2)
5. MULTIPLE ROW FAILURES	12	(10)	21	(6)	11	(3)	14	(4)	51	(13)	29	(9)	21	(7)
6. ROW PAIRS	8	(8)	16	(4)	10	(2)	9	(3)	38	(10)	28	(8)	18	(5)
7. ROW TRIPS	3	(3)	5	(1)	1	(0)	3	(1)	9	(2)	1	(0)	3	(1)
8. >3 ROWS	0	(0)	0	(0)	0	(0)	2	(1)	4	(1)	0	(0)	0	(0)
9. COLUMN FAILURES	13	(11)	82	(22)	72	(17)	52	(14)	95	(25)	42	(12)	59	(18)
10. SINGLE FULL COLUMNS	12	(10)	74	(20)	68	(16)	52	(14)	80	(21)	38	(11)	54	(16)
11. WEAK FULL COLUMNS	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
12. SINGLE HALF COLUMNS	1	(1)	2	(1)	0	(0)	3	(1)	5	(1)	1	(0)	1	(0)
13. WEAK HALF COLUMNS	0	(0)	2	(1)	0	(0)	0	(0)	2	(1)	3	(1)	1	(0)
14. MULTIPLE COLUMN FAILURES	2	(2)	4	(1)	4	(1)	15	(4)	13	(3)	16	(5)	5	(2)
15. ADJ FULL COLUMNS	1	(1)	3	(1)	3	(1)	14	(4)	7	(2)	12	(4)	4	(1)
16. ADJ WEAK COLUMNS	0	(0)	0	(0)	0	(0)	0	(0)	1	(0)	0	(0)	0	(0)
17. ADJ HALF COLUMNS	0	(0)	0	(0)	0	(0)	1	(0)	1	(0)	0	(0)	0	(0)
18. ADJ WEAK HALF COLUMNS	0	(0)	1	(0)	0	(0)	0	(0)	3	(1)	1	(0)	0	(0)
19. ADJACENT BITS	5	(4)	37	(10)	20	(5)	18	(5)	36	(9)	44	(13)	28	(8)
20. ADJ BITS (MP)	0	(0)	5	(1)	1	(0)	1	(0)	5	(1)	3	(1)	1	(0)
21. 2 PR ADJ BITS (MP)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	1	(0)	0	(0)
22. ADJ BITS (MW/GS)	3	(2)	16	(4)	10	(2)	5	(1)	26	(7)	7	(2)	15	(5)
23. 2 PR ADJ BITS (MW/GS)	0	(0)	8	(2)	2	(0)	2	(0)	5	(1)	2	(1)	3	(1)
24. ADJ BITS (GS-DW)	0	(0)	1	(0)	2	(0)	0	(0)	1	(0)	0	(0)	1	(0)
25. ADJ BITS (GS-BB)	0	(0)	1	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
26. SINGLE BITS (GS/GO)	7	(6)	17	(4)	27	(6)	24	(6)	20	(5)	17	(5)	19	(5)
27. POLY II ROW SHORT	0	(0)	0	(0)	2	(0)	0	(0)	0	(0)	1	(0)	0	(0)
28. ROW/COL POLY II SHORT	0	(0)	0	(0)	1	(0)	0	(0)	0	(0)	0	(0)	0	(0)
29. ROW DECODER	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
30. COLUMN DECODER	2	(2)	0	(0)	3	(1)	1	(0)	1	(0)	3	(1)	1	(0)
31. HALF COLUMN DECODER	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
32. URGOS	2	(2)	12	(3)	7	(2)	5	(1)	16	(4)	13	(4)	9	(3)

ELECTRICAL FAILURE ANALYSIS - # (%) OF TOTAL ANALYZABLE CHIPS

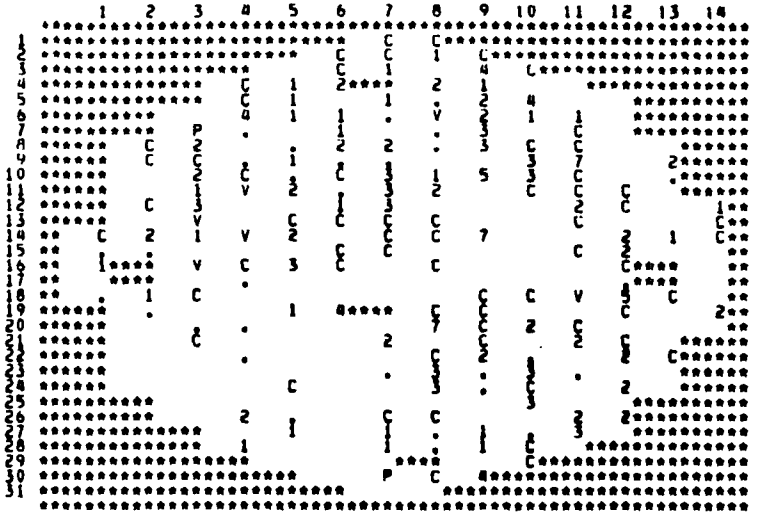
1. ROW FAILURES	7	(13)	10	(9)	8	(6)	8	(7)	19	(12)	16	(11)	11	(10)
2. SINGLE ROWS	2	(4)	5	(4)	6	(6)	3	(3)	2	(1)	6	(4)	5	(4)
3. WEAK ROWS	2	(4)	1	(1)	1	(1)	0	(0)	1	(1)	5	(3)	2	(2)
4. ROW OPENS	3	(5)	5	(4)	1	(1)	5	(5)	17	(12)	9	(6)	6	(5)
5. MULTIPLE ROW FAILURES	12	(22)	21	(19)	11	(12)	14	(13)	51	(37)	29	(20)	21	(19)
6. ROW PAIRS	8	(15)	16	(14)	10	(11)	9	(8)	38	(28)	28	(19)	18	(16)
7. ROW TRIPS	3	(5)	5	(4)	1	(1)	3	(3)	9	(7)	1	(1)	3	(3)
8. >3 ROWS	0	(0)	0	(0)	0	(0)	2	(2)	4	(3)	0	(0)	0	(0)
9. COLUMN FAILURES	13	(24)	82	(73)	72	(77)	52	(48)	95	(69)	42	(29)	59	(53)
10. SINGLE FULL COLUMNS	12	(22)	74	(65)	68	(73)	52	(48)	80	(58)	38	(26)	54	(48)
11. WEAK FULL COLUMNS	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
12. SINGLE HALF COLUMNS	1	(2)	2	(2)	0	(0)	3	(3)	5	(4)	1	(1)	1	(1)
13. WEAK HALF COLUMNS	0	(0)	2	(2)	0	(0)	0	(0)	2	(1)	3	(2)	1	(1)
14. MULTIPLE COLUMN FAILURES	2	(4)	4	(4)	4	(4)	15	(14)	13	(9)	16	(11)	5	(4)
15. ADJ FULL COLUMNS	1	(2)	3	(3)	3	(3)	14	(13)	7	(5)	12	(8)	4	(4)
16. ADJ WEAK COLUMNS	0	(0)	0	(0)	0	(0)	0	(0)	1	(1)	0	(0)	0	(0)
17. ADJ HALF COLUMNS	0	(0)	0	(0)	0	(0)	1	(1)	1	(1)	0	(0)	0	(0)
18. ADJ WEAK HALF COLUMNS	0	(0)	1	(1)	0	(0)	0	(0)	3	(2)	1	(1)	0	(0)
19. ADJACENT BITS	5	(9)	37	(33)	20	(22)	18	(17)	36	(26)	44	(30)	28	(25)
20. ADJ BITS (MP)	0	(0)	5	(4)	1	(1)	1	(1)	5	(4)	3	(2)	1	(1)
21. 2 PR ADJ BITS (MP)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	1	(1)	0	(0)
22. ADJ BITS (MW/GS)	3	(5)	16	(14)	10	(11)	5	(5)	26	(19)	7	(5)	15	(14)
23. 2 PR ADJ BITS (MW/GS)	0	(0)	8	(7)	2	(2)	2	(2)	5	(4)	2	(1)	3	(3)
24. ADJ BITS (GS-DW)	0	(0)	1	(1)	2	(2)	0	(0)	1	(1)	0	(0)	1	(1)
25. ADJ BITS (GS-BB)	0	(0)	1	(1)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
26. SINGLE BITS (GS/GO)	26	(47)	77	(68)	84	(90)	91	(83)	93	(68)	81	(56)	75	(67)
27. POLY II ROW SHORT	0	(0)	2	(2)	2	(2)	0	(0)	0	(0)	1	(1)	0	(0)
28. ROW/COL POLY II SHORT	0	(0)	0	(0)	1	(1)	0	(0)	0	(0)	0	(0)	0	(0)
29. ROW DECODER	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
30. COLUMN DECODER	2	(4)	0	(0)	3	(3)	1	(1)	1	(1)	3	(2)	1	(1)
31. HALF COLUMN DECODER	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)	0	(0)
32. URGOS	2	(4)	12	(11)	7	(8)	5	(5)	16	(12)	13	(9)	9	(8)
33. PRE-SCREEN ELIMINATION	1	(2)	5	(4)	7	(8)	5	(5)	11	(8)	4	(3)	4	(4)
34. TOO COMPLEX	35	(64)	61	(54)	75	(81)	83	(76)	17	(12)	46	(32)	58	(52)

THE DEFECT TYPES USED FOR THIS RUN ARE = 26

5 INCH WAFER MAP FOR WAFER # = 42
ANALYZABLE CHIPS = 55

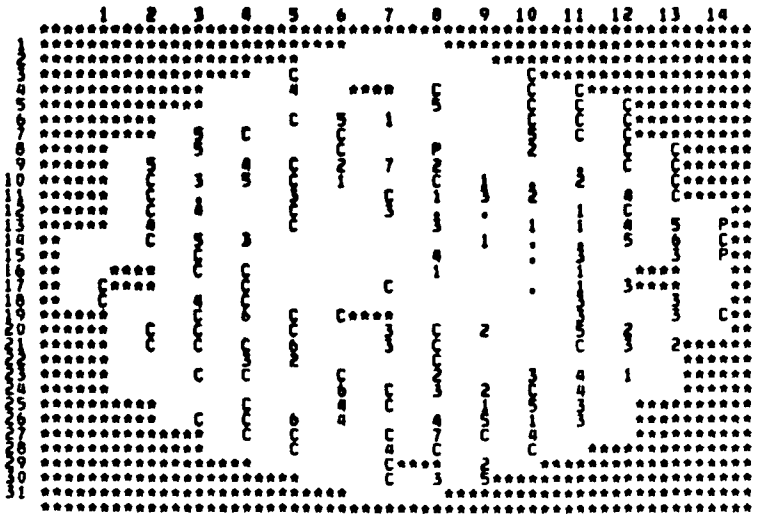


5 INCH WAFER MAP FOR WAFER # = 02
ANALYZABLE CHIPS = 113

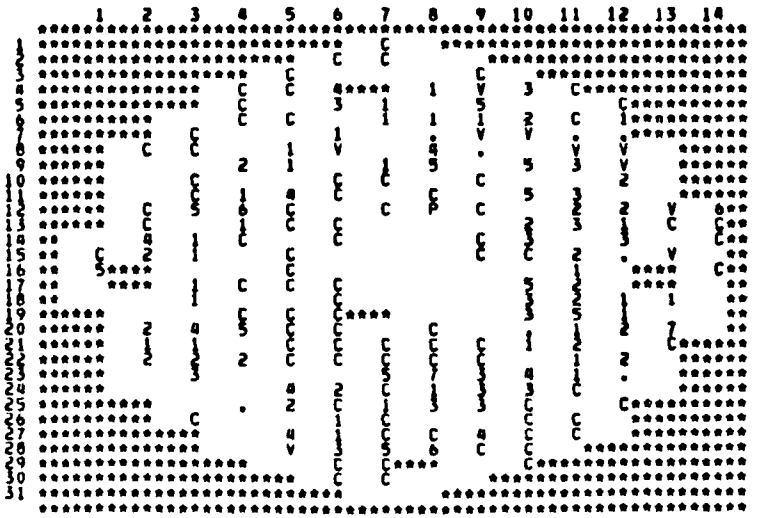


"SPACE" = NO INFORMATION FOR THIS SITE
"#" = NUMBER OF OCCURENCES FOR SELECTED DEFECT
"." = ZERO OCCURENCES OF SELECTED DEFECT
"*" = SITE WAS TOO COMPLEX TO ANALYZE
"P" = SITE SCREENED BEFORE ANALYSIS (PRE-SCREENED)

5 INCH WAFER MAP FOR WAFER # = 44
ANALYZABLE CHIPS = 93



5 INCH WAFER MAP FOR WAFER # = 37
ANALYZABLE CHIPS = 109



111 DEFECT TYPES USED FOR THIS RUN ARE = 26

5 INCH WAFER MAP FOR WAFER # = 42
ANALYZABLE CHIPS = 55

5 INCH WAFER MAP FOR WAFER # = 02
ANALYZABLE CHIPS = 113

"SPACE" = NO INFORMATION FOR THIS SITE
"#" = NUMBER OF OCCURENCES FOR SELECTED DEFECT
"." = ZERO OCCURENCES OF SELECTED DEFECT
"C" = SITE WAS TOO COMPLEX TO ANALYZE
"P" = SITE SCREENED BEFORE ANALYSIS (PRE-SCREENED)

5 INCH WAFER MAP FOR WAFER # = 44
ANALYZABLE CHIPS = 93

5 INCH WAFER MAP FOR WAFER # = 37
ANALYZABLE CHIPS = 109

THE DEFECT TYPES USED FOR THIS RUN ARE - 26
5 INCH WAFER MAP FOR WAFER # - 07
ANALYZABLE CHIPS = 157
5 INCH WAFER MAP FOR WAFER # - 05
ANALYZABLE CHIPS = 165
"SPACE" = NO INFORMATION FOR THIS SITE
"0" = NUMBER OF OCCURENCES FOR SELECTED DEFECT
"." = ZERO OCCURENCES OF SELECTED DEFECT
"&" = SITE WAS TOO COMPLEX TO ANALYZE
"S" = SITE SCREENED BEFORE ANALYSIS (PRE-SCREENED)

1

THE DEFECT TYPES USED FOR THIS RUN ARE - 26

5 INCH WAFER MAP FOR WAFER # - 07
ANALYZABLE CHIPS = 157

5 INCH WAFER MAP FOR WAFER # - 05
ANALYZABLE CHIPS = 145

"BSPACE" = NO INFORMATION FOR THIS SITE
"#" = NUMBER OF OCCURENCES FOR SELECTED DEFECT
. = ZERO OCCURENCES OF SELECTED DEFECT
C = SITE WAS TOO COMPLEX TO ANALYZE
P = SITE SCREENED BEFORE ANALYSIS (PRE-SCREENED)

APPENDIX C
Random Sample
(Raw Data)

Wafer: Site	42	02	44	37	07	05
25.3	-	-	-	-	-	0
9.12	-	-	-	0	-	0
29.6	-	-	-	-	2	-
14.1	-	-	-	-	-	-
17.5	-	-	-	-	-	-
12.13	0	-	-	0	0	-
23.2	-	-	-	-	-	-
8.7	-	2	-	-	1	-
7.3	-	-	5	-	-	-
14.2	-	2	-	4	0	-
5.9	-	2	-	5	-	1
13.3	-	0	-	-	0	-
28.7	1	1	4	5	0	0
6.4	-	4	-	-	2	0
23.7	-	0	-	5	-	-
23.2	-	-	-	-	-	-
13.6	-	-	-	-	-	5
16.11	0	-	1	1	4	0
19.6	-	4	-	-	1	-
21.5	-	-	3	-	0	1
18.8	-	-	-	-	0	-
11.9	-	-	3	-	0	-
13.4	-	-	-	1	-	0
2.8	-	1	-	-	1	-
26.3	-	-	-	-	-	-
18,1	0	0	-	-	-	-
11.12	-	-	4	-	0	-
16.1	-	1	-	5	-	-

Wafer: Site	42	02	44	37	07	05
14.8	-	-	-	-	-	-
31.8	-	-	-	-	-	-
5.6	-	-	-	3	0	0
20.7	-	-	3	-	-	4
5.5	-	1	-	-	-	0
8.3	-	2	5	-	-	-
15.3	-	-	-	1	-	-
19.2	-	0	-	-	-	-
10.4	-	-	5	-	0	0
16.3	-	0	-	-	-	-
22.11	-	-	-	1	1	-
8.13	-	-	-	-	-	-
25.3	-	-	-	-	-	0
4.5	-	1	4	-	-	4
24.3	-	-	-	-	-	-
17.8	-	-	-	-	-	-
23.9	-	0	-	3	3	-
11.8	-	2	1	-	3	-
24.12	-	2	-	-	-	-
13.12	-	-	4	1	1	-
20.3	-	0	-	4	2	-
21.8	-	-	-	-	-	2
24.11	0	-	4	-	2	0
20.10	-	2	-	0	0	-
28.9	-	1	-	-	-	1
22.2	-	-	-	2	-	1
23.4	5	-	-	-	0	-
Total	6	28	46	40	23	19
Sites	6	22	13	17	24	19

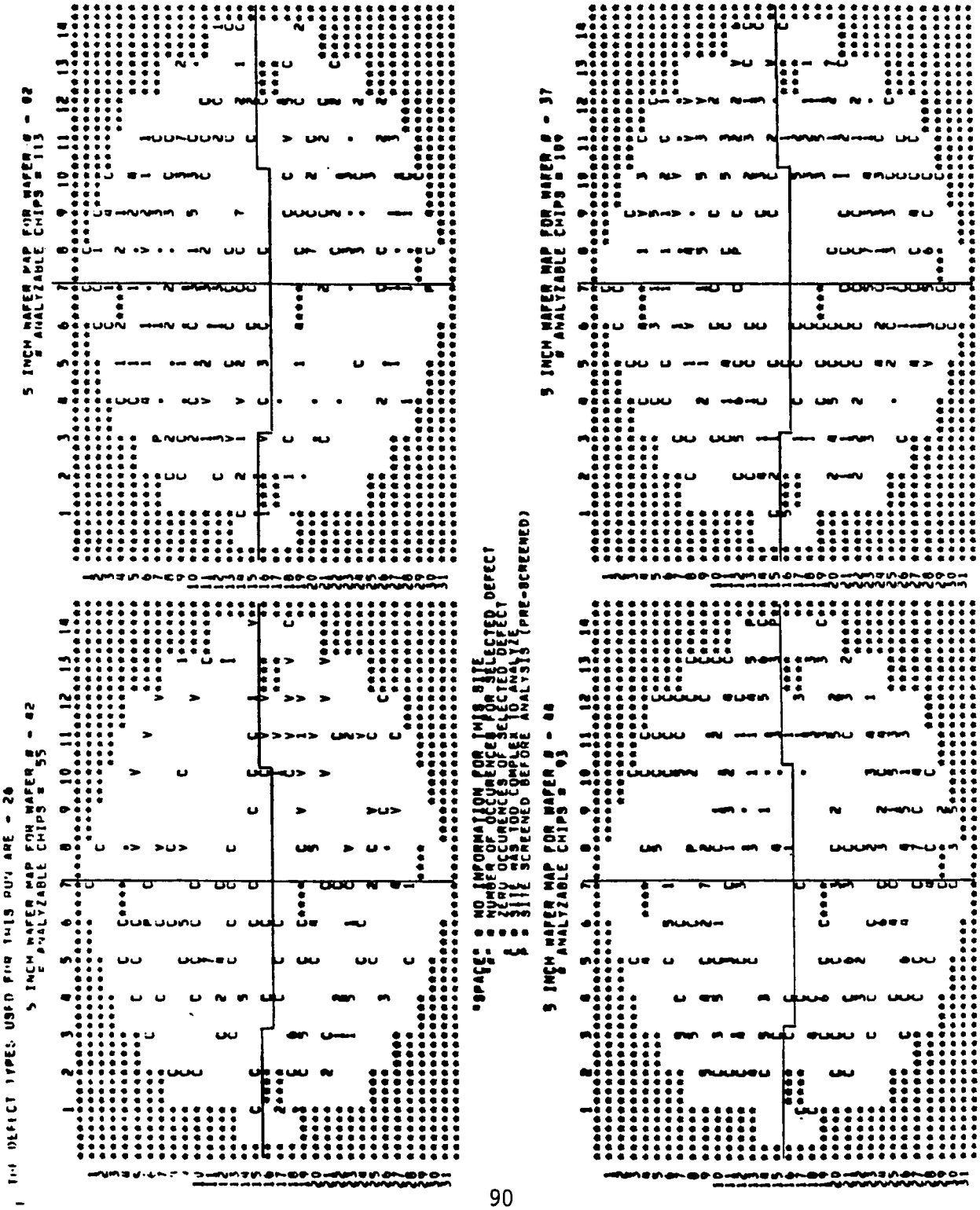
APPENDIX D

Radial Stratified Sample (Raw Data)

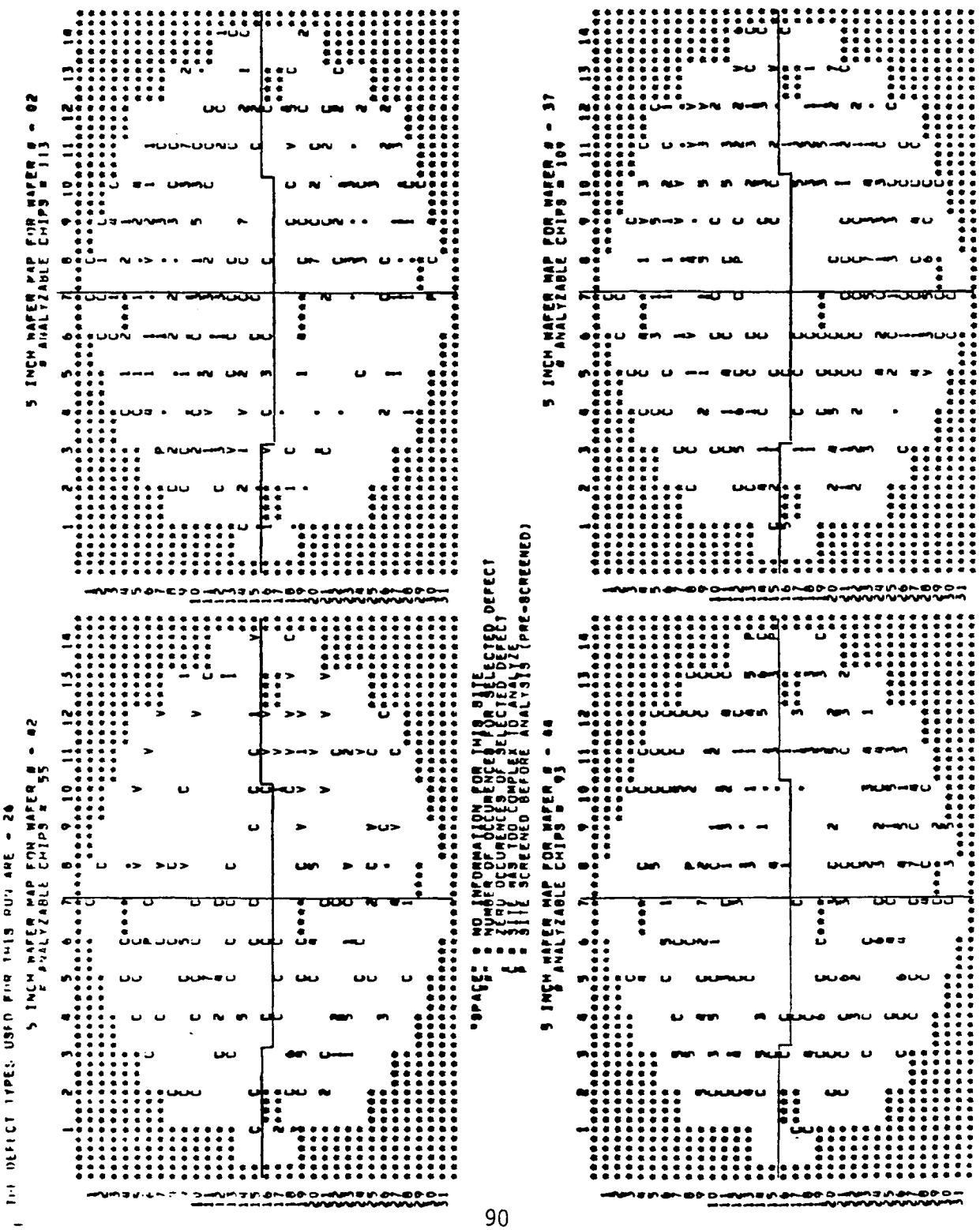
Wafer: Site	42	02	44	37	07	05
25.3	-	-	-	-	-	0
9.12	-	-	-	0	-	0
29.6	-	-	-	-	2	-
14.1	-	-	-	-	-	-
17.5	-	-	-	-	-	-
12.13	0	-	-	0	0	-
23.2	-	-	-	-	-	-
8.7	-	2	-	-	1	-
7.3	-	-	5	-	-	-
14.2	-	2	-	4	0	-
5.9	-	2	-	5	-	1
13.3	-	0	-	-	0	-
28.7	1	1	4	5	0	0
6.4	-	4	-	-	2	0
23.7	-	0	-	5	-	-
23.2	-	-	-	-	-	-
13.6	-	-	-	-	-	5
16.11	0	-	1	1	4	0
19.6	-	4	-	-	1	-
21.5	-	-	3	-	0	1
18.8	-	-	-	-	0	-
11.9	-	-	3	-	0	-
13.4	-	-	-	1	-	0
2.8	-	1	-	-	1	-
26.3	-	-	-	-	-	-
18.1	0	0	-	-	-	-
11.12	-	-	4	-	0	-
16.1	-	1	-	5	-	-

Wafer: Site	42	02	44	37	07	05
14.8	-	-	-	-	-	-
31.8	-	-	-	-	-	-
5.6	-	-	-	3	0	0
20.7	-	-	3	-	-	4
5.5	-	1	-	-	-	0
8.3	-	2	5	-	-	-
15.3	-	-	-	1	-	-
19.2	-	0	-	-	-	-
10.4	-	-	5	-	0	0
16.3	-	0	-	-	-	-
22.11	-	-	-	1	1	-
8.13	-	-	-	-	-	-
25.3	-	-	-	-	-	0
4.5	-	1	4	-	-	4
23.9	-	0	-	3	3	-
11.8	-	2	1	-	3	-
13.12	-	-	4	1	1	-
20.3	-	0	-	4	2	-
21.8	-	-	-	-	-	2
24.11	0	-	4	-	2	0
20.10	-	2	-	0	0	-
23.4	5	-	-	-	0	-
22.3	1	-	-	2	0	-
12.12	-	-	-	2	0	-
22.5	-	-	2	-	0	0
13.11	-	-	1	3	-	-
23.5	-	-	-	-	-	0
Total	7	25	49	45	23	17
Sites	7	22	15	20	27	21

Appendix E (1 of 2)
Wafer Map Showing
Quadrant Stratification

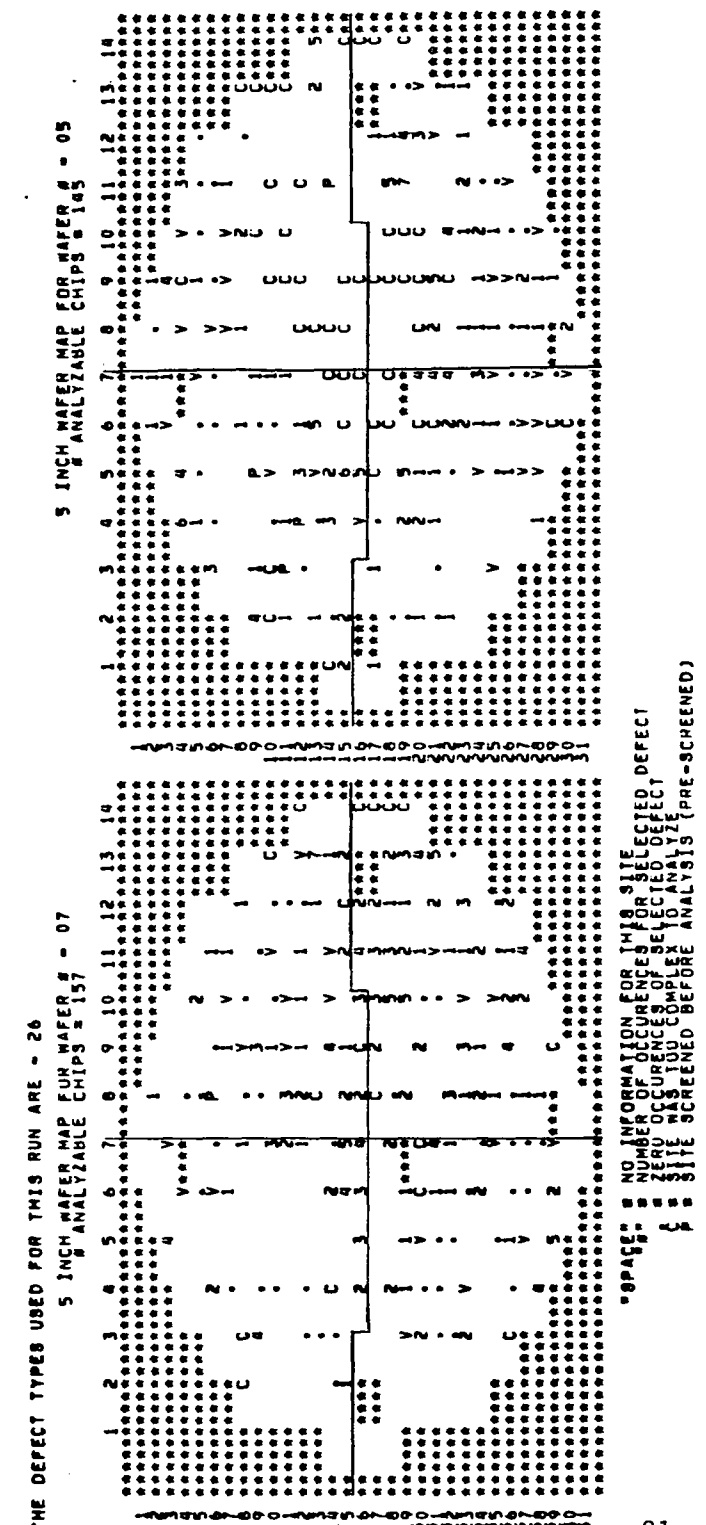


Appendix E (1 of 2)
Wafer Map Showing
Quadrant Stratification



Appendix E (2 of 2)
Wafer Map Showing
Quadrant Stratification

Appendix E (2 of 2)
Wafer Map Showing
Quadrant Stratification



APPENDIX F

Stratified Systematic Sampling (Quadrants)
(Raw Data)

	QUAD	SUMX	SUM_X^2	#ANAL	1	2	3	4	5	6	7	8	9	10	11	12	13
42	1	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-
	2	8	24	3	-	-	-	-	2	-	-	-	-	-	-	4	2
	3	3	5	3	-	-	-	-	1	-	-	2	0	-	-	-	-
	4	1	1	3	-	0	-	-	-	-	-	-	-	-	0	1	-
02	1	9	17	7	2	-	1	-	0	-	1	-	1	1	-	3	-
	2	1	1	4	0	-	0	-	0	-	-	-	-	-	-	1	-
	3	7	17	4	-	3	-	-	-	-	2	-	2	-	0	-	-
	4	4	16	2	0	-	-	-	4	-	-	-	-	-	-	-	-
44	1	16	90	4	-	-	0	-	4	-	-	-	-	5	-	7	-
	2	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	19	79	5	-	4	5	2	-	5	-	-	-	-	-	3	-
	4	11	33	6	-	2	4	0	-	-	0	-	2	-	-	3	-
37	1	2	2	3	-	-	1	-	-	1	-	-	-	0	-	-	-
	2	13	49	4	-	2	-	-	-	4	-	-	2	-	5	-	-
	3	15	67	5	-	7	-	-	-	3	-	-	2	-	2	-	1
	4	11	45	6	-	-	-	-	0	2	-	-	0	1	2	-	6
07	1	5	7	6	1	-	-	2	0	-	-	-	-	1	-	1	0
	2	5	9	8	-	-	-	2	-	0	0	0	0	1	2	0	-
	3	11	23	8	0	2	-	-	-	0	2	1	1	2	3	-	-
	4	7	11	7	-	-	-	4	0	-	0	0	1	1	1	-	-
05	1	7	9	7	2	-	1	-	1	1	-	0	-	1	1	-	-
	2	7	19	7	0	-	0	-	1	-	-	-	-	1	4	0	1
	3	14	58	8	-	0	1	-	-	4	0	0	5	4	-	0	-
	4	3	5	5	-	0	-	1	-	-	-	2	0	-	0	-	-

Quad	N	Sumx	$Sumx^2$
1	27	39	125
2	26	34	102
3	33	69	249
4	29	37	111

APPENDIX G

Straight Systematic Sampling
(Every Fifth Site)

Start Site #	5	1	1	3	4	5							
Wafer	42	02	44	37	07	05		42	02	44	37	07	05
1	0	-	-	-	-	-	30	-	-	-	6	0	0
	-	-	-	2	-	1		-	-	4	7	1	1
	-	0	-	-	0	1		-	0	-	-	1	-
	-	-	-	-	-	-		-	-	-	-	0	-
	-	-	-	-	4	-		-	-	4	4	-	-
	-	1	0	-	0	-		0	-	-	-	0	0
	-	0	-	1	0	-		-	0	5	0	-	0
	-	-	-	-	-	0		-	1	-	-	-	1
	-	-	-	-	0	-		-	2	-	-	3	-
10	-	-	-	-	0	2		-	5	1	-	4	-
	-	-	6	1	2	-	40	-	-	2	3	-	-
	-	0	3	-	-	0		0	-	1	-	1	-
	-	0	4	-	2	1		-	-	5	-	-	-
	-	-	-	1	-	-		-	4	5	0	2	1
	7	1	-	-	-	-		-	3	-	-	0	-
	-	2	-	-	-	5		-	2	0	-	3	-
	-	3	-	-	0	1		-	-	0	-	0	-
	-	-	2	0	0	1		0	3	-	-	-	0
	-	0	-	1	-	-		0	4	-	3	-	0
20	-	-	-	-	-	1		-	1	1	1	0	-
	-	-	-	-	-	-	50	0	-	3	2	2	-
	-	4	-	-	4	-		-	-	4	-	1	-
	5	-	-	1	-	0		-	2	-	-	0	0
	-	0	-	-	0	-		-	2	-	2	2	-
	-	2	-	1	-	1		-	-	2	0	2	3
	-	1	-	-	1	1		1	-	-	2	2	-
	-	0	-	-	-	-		0	2	-	-	0	-
	-	-	3	-	2	4		-	-	-	0	-	0
	2	-	-	-	0	0		0	-	-	-	-	-
								-	-	3	-	2	0
							60	-	-	-	-	-	-
								-	-	-	-	-	-
# Anal Sites								12	28	21	21	36	28
Sumx =								15	45	58	38	41	25
Sum^2 =								79	133	226	142	107	65

Appendix H

PROPOSED LOT SUMMARY

	1	2	3	4	5	6	7	8	9	10	
Lot	5084	5086	5088	5089	5090	5091	5092	5093	5094	5095	Sum
# Wafers	15	12	21	20	22	18	17	17	15	19	176
Analyzable/Wafer	55	113	93	109	157	145	26	126	143	182	117
# Virgin/Wafer	25	6	0	10	20	26	0	16	19	31	15
# Diag Dead/Wafer	85	53	64	46	57	46	30	47	36	37	50
# Repairable/Wafer	44	108	109	121	131	123	97	110	133	165	116
# Failures/Wafer	120	373	414	360	382	341	153	335	375	423	333
# Failures/Anal. Site	2.18	3.30	4.45	3.30	2.43	2.35	5.88	2.66	2.62	2.32	2.85
Approximate Yield/Wafer	64	103	98	118	137	136	97	126	152	196	124

PERCENT OF TOTAL FAILURES

											r	r^2	Rank
A	Row Failures	7	3	2	2	5	6	1	5	1	1	-.386	.149	1
B	Multiple Row Failures	10	6	3	4	13	9	3	4	4	8	.132	.017	2
C	Column Failures	11	22	17	16	9	12	1	22	12	14	.068	.005	7
D	Multiple Column Failures	2	9	3	4	3	5	1	6	2	2	.101	.010	4
E	Adjacent Bits	5	10	5	5	9	13	3	4	5	6	.183	.033	3
F	Single Bits	62	46	67	67	54	50	91	54	71	67	-.059	.003	8
G	Unrecognizable	2	3	2	1	4	4	0	1	3	1	.099	.010	4
H	Other	1	1	1	1	3	1	0	4	2	1	.244	.060	6

PERCENT OF ANALYZABLE SITES

I	Row Failures	13	9	6	7	12	11	8	10	2	3	-.585	.343	2
J	Multiple Row Failures	20	16	11	12	26	19	15	11	10	3	-.495	.245	4
K	Column Failures	15	54	54	31	20	23	8	40	27	26	-.042	.002	8
L	Multiple Column Failures	4	25	13	13	8	10	4	13	5	5	-.194	.038	5
M	Adjacent Bits	11	27	16	13	21	24	12	10	13	12	-.015	.0002	9
N	Single Bits	47	68	90	83	59	56	100	65	71	60	-.187	.035	6
O	Unrecognizable	4	11	8	5	10	8	0	3	6	2	-.079	.006	7
P	Pre-Screen	1	1	2	1	1	2	1	1	0	0	-.527	.277	3
Q	Too Complex	54	35	44	43	10	24	87	18	31	18	-.635	.404	1

Appendix I

ANOVA TO SHOW DIFFERENCES BETWEEN LOT SERIES

Category		Sumx	$Sumx^2$	T	C	SST	SS(TR)	SSE	Source	ss	df	ms	f
A	a	19	91	33	108.9	46.1	2.5	43.6	Lot Series	2.5	1	2.5	0.5
	b	14	64						Error	43.6	8	5.5	
									Total	46.1	9		
B	a	36	330	64	409.6	106.4	6.4	100.0	Lot Series	6.4	1	6.4	0.5
	b	28	186						Error	100.0	8	12.5	
									Total	106.4	9		
C	a	75	1231	136	1849.6	350.4	19.6	330.8	Lot Series	19.6	1	19.6	0.5
	b	61	969						Error	330.8	8	41.4	
									Total	350.4	9		
D	a	21	119	37	136.9	52.1	2.5	49.6	Lot Series	2.5	1	2.5	0.4
	b	16	70						Error	49.6	8	6.2	
									Total	52.1	9		
E	a	34	256	65	422.5	88.5	0.9	87.6	Lot Series	0.9	1	0.9	0.1
	b	31	255						Error	87.6	8	11.0	
									Total	88.5	9		
F	a	296	17854	629	39564.1	1516.9	136.9	138.0	Lot Series	136.9	1	136.9	0.8
	b	333	23227						Error	138.0	8	172.5	
									Total	1516.9	9		

$F_{0.05} = 5.32$

"a" denotes lot series "a"
"b" denotes lot series "b"

Vita

The author was born on April 1, 1957, in Summit, New Jersey, to Mr. and Mrs. Alan G. Chynoweth. He received his primary education through the Summit public school system. The author pursued his BS in Industrial Engineering at Lehigh University in Bethlehem, Pennsylvania, during the years 1975 through 1979.

Upon graduation, Kevin Chynoweth joined Western Electric's Allentown Works in 1979 as a member of the Production Control organization where he had spent his summer of 1978 as a summer employee. The activities pursued within this organization include the study of operation research techniques to aid in production control activities.

After a two-year tour of duty in that organization a transfer was made to the company's Information Systems Department for a one-year period. In this position the author was involved in the early design stages of a major division-wide shop floor control computer system.

In August of 1981 Kevin Chynoweth was transferred into a Development Engineering Department where he spent the next two and a half years developing computer data links and analysis systems networked with memory device test equipment. Kevin served as the computer system manager of two DEC PDP 11/44 computer systems before being reclassified in April 1984 to a Supervisor in the Manufacturing Planning and Control Department. Kevin is currently responsible for all planning and control functions pertaining to AT&T Technologies' MOS Assembly and Test manufacturing line.